## Features and Benefits

Low Power Supply Voltage: 3.3, 2.5 V supply options Clock Output: LVPECL
Output frequency support from 15 MHz to 2.1 GHz
Ultra Low Noise, Phase Jitter < 300 fs
(Typical: 150 fs at 12 kHz to 20 MHz frequency offsets)
Tri-state enable / disable mode.
Temperature Range: $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
Pb-free/RoHS Compliant

## Typical Applications

SONET/SDH,. Gigabit Ethernet.

- Storage Area Networking (SAN)
- SD/HD video
- FPGA clock generation


## Mechanical Drawing \& Pin Connections


[SIDE VIEW]

[ BOTTOM VIEW ]


| PIN\# | FUNCTION |
| :---: | :--- |
|  | LVPECL/LVDS/CML/HCSL |
| 1 | NC |
| 2 | OE |
| 3 | GND |
| 4 | Output |
| 5 | Comp.Output |
| 6 | VDD |
| 7 | NC |
| 8 | NC |

Unit in mm
$1 \mathrm{~mm}=0.0394$ inches

## Specifications

| Specification | Condition | 3.3 V |  | 2.5 V |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Max. | Min. | Max. |  |
| Supply Voltage Variation |  | V do-10\% | V dot $10 \%$ | V do-10\% | V ${ }_{\text {d }}+10 \%$ | V |
| Frequency Range |  | 15 | 2100 | 15 | 2100 | MHz |
| Standard Frequency |  | $\begin{aligned} & 100,106.25, \\ & 300,312.5, \end{aligned}$ | 25, 156.25 <br> 0, 491.52, | $\begin{aligned} & 187.5,200, \\ & 22.08,644.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 212.5,266, \\ & 31250 \end{aligned}$ | MHz |
| Supply Current |  | - | 110 | - | 95 | mA |
| Duty Cycle |  | 45 | 55 | 45 | 55 | \% |
| Output Level | Output High | V do-1.165 | V do-0.8 | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{DD}}- \\ & 1.165 \end{aligned}$ | V do-0.8 | v |
|  | Output Low | V do-2.0 | V do-1.55 | V do-2.0 | V DD-1.55 |  |
| Transition Rise/Fall Time |  | - | 0.35 | - | 0.35 | nSec |
| Start Time |  | - | 8 | - | 8 | mSec |
| Tri-State(Input to Pin2) | Enable | 0.7 VV do | - | 0.7 xV do | - | v |
|  | Disable | - | $0.3 \times \mathrm{V}$ D | - | 0.3 xV do |  |
| Standby Current |  | - | 110 | - | 95 | mA |
| RMS Phase Jitter (12KHz to 20MHz) |  | 150 | 300 | 150 | 300 | fs |
| Period Jitter |  | - | 50 | - | 50 | ps |
| Phase Noise, At $\mathrm{V}_{\mathrm{DD}}=3.3 \mathrm{~V}$, fout $=873.515 \mathrm{MHz}$ |  | TYP | MAX | TYP | MAX |  |
|  | 1 KHz offset | -106 | - | -106 |  | dBc/Hz |
|  | 10 KHz offset | -115 | - | -115 |  | dBc/Hz |
|  | $100 \mathrm{KHz}$ offset | -123 | - | -123 |  | dBc/Hz |
|  | 1 MHz offset | -133 | - | -133 |  | dBc/Hz |
|  | 20 MHz offset | -150 | - | -150 |  | dBc/Hz |

## Frequency Stability vs. Temperature

|  | $\mathbf{\pm 2 0 P P M}$ | $\mathbf{\pm 2 5 P P M}$ | $\mathbf{\pm 3 0 P P M}$ | $\mathbf{\pm 5 0 P P M}$ |
| :---: | :---: | :---: | :---: | :---: |
| $-20^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Conditional | Available | Available | Available |
| $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | Not Available | Conditional | Available | Available |

Note: Inclusive of calibration @ $25^{\circ} \mathrm{C}$, operating temperature range, input voltage variation, load variation, aging ( $1^{\text {st }}$ year), shock and vibration.

