



Features and Benefits

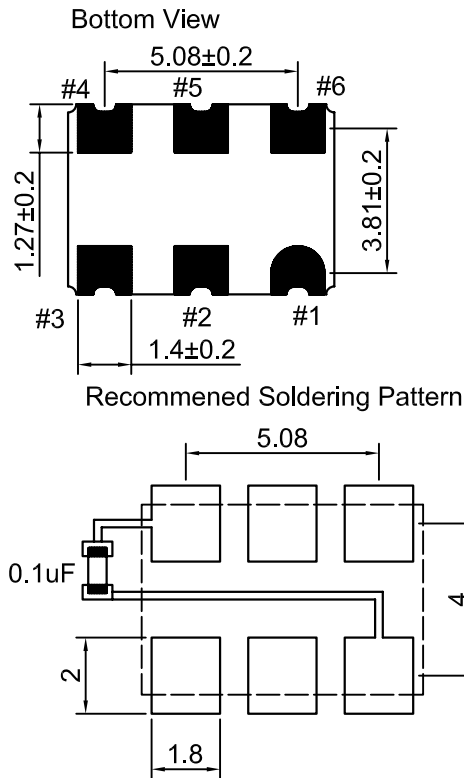
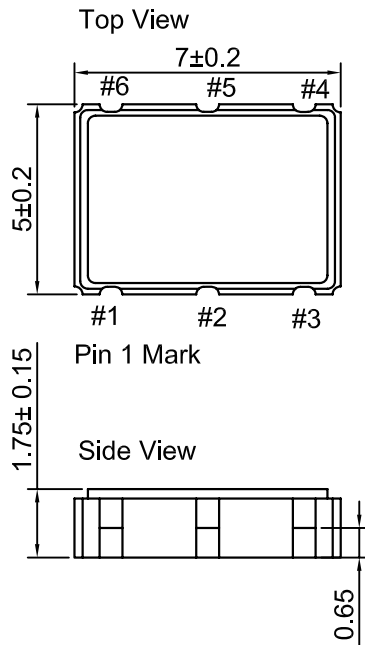
- Typical 7.0x5.0x1.75 mm ceramic SMD package
- Low jitter performance
- Wide frequency control voltage
- Complementary output
- Tri state enable/disable

Typical Applications

- Set-top Box, HDTV, WiMAX/WLAN,
- xDSL/VoIP, Cable Modem

Mechanical Drawing & Pin Connections

Drawing No: MD150035-1



Pin Functions

Pin	Function
#1	Vcon
#2	Tri-State
#3	GND
#4	Output
#5	Comp.Output/NC
#6	VDD

Unit in mm
1mm = 0.0394 inches

PIN#5 Note: N.C. for CMOS
Comp. Output for LVPECL/LVDS



CMOS Specifications

Specification	Conditon	3.3V		Unit
		Min.	Max.	
Supply Voltage Variation	$V_{DD} \pm 5\%$	3.135	3.465	V
Frequency Range		1.5	170	MHz
Standard Frequency	10, 20, 25, 27, 32.768, 35.328, 38.88, 61.44, 122.88, 153.6			MHz
Supply Current	$1.5\text{MHz} \leq F_o < 20\text{MHz}$	-	10	mA
	$20\text{MHz} \leq F_o < 50\text{MHz}$	-	20	
	$50\text{MHz} \leq F_o \leq 80\text{MHz}$	-	30	
	$80\text{MHz} < F_o < 160\text{MHz}$	-	40	
	$160\text{MHz} \leq F_o \leq 170\text{MHz}$	-	50	
Control Voltage		0.3	3.0	V
Absolute Pulling Range		± 50	-	ppm
Output Level(CMOS)	Output High	2.97	-	V
	Output Low	-	0.33	
Transition Rise/Fall Time*	$1.5\text{MHz} \leq F_o < 20\text{MHz}$	-	5	nSec
	$20\text{MHz} \leq F_o < 50\text{MHz}$	-	4	
	$50\text{MHz} \leq F_o \leq 80\text{MHz}$	-	3	
	$80\text{MHz} < F_o \leq 170\text{MHz}$	-	2	
Start Time		-	5	mSec
Tri-State(Input to Pin2)	Enable (High voltage or floating)	2.31	-	V
	Disable (Low voltage or GND)	-	0.99	
Period Jitter(Pk-Pk)		-	40	pSec
RMS Phase Jitter	Integrated 12KHz to 20MHz	-	1	pSec
Linearity		-	10	%
Modulation Bandwidth	$1.5\text{MHz} \leq F_o \leq 170\text{MHz}$	15	-	KHz
Input Impedance	$1.5\text{MHz} \leq F_o \leq 170\text{MHz}$	10000	-	Kohm
Phase Noise@30.72MHz	100Hz	-115		dBc/Hz
	1KHz	-135		
	10KHz	-150		
Aging	@25°C 1 st year	-	± 3	ppm
Storage Temp. Range		-55°C to +125°C		

Note: *Transition times are measured between 10% and 90% of V_{DD} with an output load of 15pF

Frequency Stability vs. Temperature (CMOS)

	$\pm 25\text{PPM}$	$\pm 50\text{PPM}$
-10°C to +60°C	Available	Available
-20°C to +70°C	Available	Available
-40°C to +85°C	Conditional	Available



LVPECL/LVDS Specifications

Specification	Conditon	LVPECL				LVDS				Unit
		3.3V		2.5V		3.3V		2.5V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation	$V_{DD} \pm 5\%$	3.135	3.465	2.375	2.625	3.135	3.465	2.375	2.625	V
Frequency Range		1.5	200	65	200	1.5	200	65	200	MHz
Standard Frequency		77.76, 106.25, 122.88, 125, 155.52, 156.25, 200								MHz
Control Voltage		0.3	3.0	0	2.5	0.3	3.0	0	2.5	V
Absolute Pulling Range		± 50	-	± 50	-	± 50	-	± 50	-	ppm
Supply Current	$1.5\text{MHz} \leq F_o < 65\text{MHz}$	-	75	-	75	-	45	-	45	mA
	$65\text{MHz} \leq F_o \leq 200\text{MHz}$	-	100	-	100	-	80	-	80	
Output Level	Output High	2.275	-	1.475	-	-	1.6	-	1.6	V
	Output Low	-	1.68	-	1.095	0.9	-	0.9	-	
Transition Rise/Fall Time*		-	1.0	-	1.0	-	1.0	-	1.0	nSec
Start Time		-	3	-	3	-	3	-	3	mSec
Tri-State(Input to Pin2, Enable High)	Enable (High voltage or floating)	2.31	-	1.75	-	2.31	-	1.75	-	V
	Disable (Low voltage or GND)	-	0.99	-	0.75	-	0.99	-	0.75	
Linearity		-	10	-	10	-	10	-	10	%
Modulation Bandwidth		15	-	15	-	15	-	15	-	KHz
Input Impedance		10000	-	10000	-	10000	-	10000	-	Kohm
RMS Phase Jitter (Integrated 12KHz to 20MHz)	$F_o < 100\text{MHz}$	-	1	-	1	-	1	-	1	pSec
	$100\text{MHz} \leq F_o < 125\text{MHz}$	-	0.7	-	0.7	-	0.7	-	0.7	
	$125\text{MHz} \leq F_o < 150\text{MHz}$	-	0.5	-	0.5	-	0.5	-	0.5	
	$150\text{MHz} \leq F_o$	-	0.3	-	0.3	-	0.3	-	0.3	
Phase Noise @153.6MHz	@100Hz	-85		-85		-85		-85		dBc/Hz
	@1KHz	-115		-115		-115		-115		
	@10KHz	-130		-130		-130		-130		
Aging	@25°C 1 st year	-	± 3	-	± 3	-	± 3	-	± 3	ppm
Storage Temp. Range		-55°C to +125°C								°C

Note: *Transition times are measured between 20% and 80% of V_{DD}

Frequency Stability vs. Temperature (LVPECL/LVDS)

	$\pm 25\text{PPM}$	$\pm 50\text{PPM}$
-10°C to +60°C	Conditional	Available
-20°C to +70°C	Conditional	Available
-40°C to +85°C	Not Available	Available