# LC!) !+!&') J!@8 G!I A < n LVDS10 to 1450MHz Clock Oscillator

### **Features and Benefits**

Frequency Range 10 MHz to 1450 MHz Output Frequency to six decimal places

Output Frequency Examples: 12.688375 MHz; 125.345678 MHz

7 mm x 5.0 mm x 1.80 mm ceramic SMD 6-pad ±50 ppm total stability over -40°C to 85°C

1 to 1.5 pico-second phase jitter ( 12KHz to 20 MHz )

LVDS outputs 2.5V supply

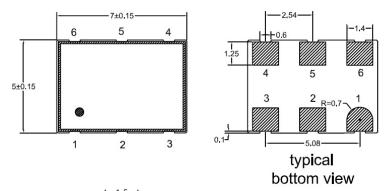
### **Typical Applications**

GbE Ethernet, SONET, Fibre channel, FPGA, and A/D clock reference devices

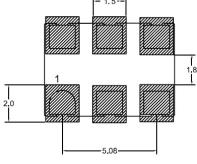
### Description

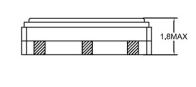
A new generation of low jitter / low power clock oscillators has been developed using the latest low noise integrated circuit topologies.

### **Mechanical Drawing & Pin Connections**



Product	ХО	VCXO	
Pad 1	High Enable Voltage Control		
Pad 2	No Connection High Enable		
Pad 3	Ground		
Pad 4	CMOS: Output LVPECL, LVDS: Differential Output		
Pad 5	CMOS: No connection LVPECL, LVDS: Complementary Output		
Pad 6	Supply voltage		







## Dynamic Engineers Inc.

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### LC!) !+!&') J!@8G!I A<n LVDS10 to 1450MHz Clock Oscillator

### **Specifications**

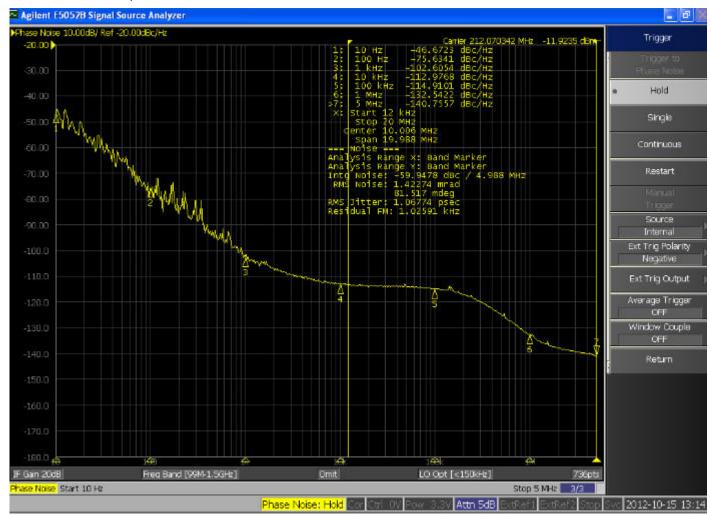
LVDS	General Specifications: at Ta=+25°C,					
Dodd	Output Logic Type		LVDS			
Power Supply Voltage (V <sub>DD</sub> )	Frequency Range		10 ~ 1450 MHz			
Output "High" Voltage (Vob)  Output "Low" Voltage; VoL  Voltage (Vob)  Integrated Phase Jitter, rms (12 KHz to 20 MHz)  Output Disable Time  Current Caps Hand  Output Disable Time  Current Agriculture (Taps Agree)  Output Disable Time  Current Agree  Output Disable Time  Current Output Disable Time  Current Output Disable Time  Current Output Disable Time  Current Output Disable Time  Output Disable Time  Current Agriculture (Taps Agree)  Output Disable Time  Current Output Disable Time  Output Disable Time  Output Disable Time  Current with Output Disable Time  Output	Load		Differential			
Output "Low" Voltage; VoL         Voltage (VoD)         1.1 V Typical , 0.9 V min.           Frequency Stability         ±50 ppm over -40°C to 85°C Over all conditions           Duty Cycle         50% ± 5%           Rise Time (Tr)/Fall Time (Tf)         0.2nS. typ. 0.4nS. max.           (20% VoD − 80% VoD)         100 MHz: 16 mA           Current Consumption VoD + 2.5 V         500 MHz: 21 mA           All values are typical and over operating temperatures.         500 MHz: 21 mA           1 GHz:24 mA         750 MHz: 22 mA           1 Gurrent with Output Disabled         16 mA typical           Start-up Time         10 ms mx.           Aging         ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years           OE Pad Input XOS: Pad 1         70% of VoB maximum to disable output (high impedance). LVCMOS/LVTTL level.           VCXOs: Pad 2         30% of VbB maximum to disable output (high impedance). LVCMOS/LVTTL level.           Output Enable Time         200 ns max.           Output Disable Time         200 ns max.           Fhase Jitter, rms (12 KHz to 20 MHz)         1.0 pS typical; 1.5 pS max.           Phase Jitter, rms (1.875 MHz to 20 MHz)         1.0 pS typical; 1.5 pS max.           ROHS Status         RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)           Storage Temp. Range </th <th colspan="2">Power Supply Voltage (V<sub>DD</sub>)</th> <th colspan="3">V<sub>DD</sub> = +2.5V D.C. ± 5%</th>	Power Supply Voltage (V <sub>DD</sub> )		V <sub>DD</sub> = +2.5V D.C. ± 5%			
South   Sou	Output "High" Voltage;	V <sub>OH</sub>	Voltage (V <sub>OD</sub> )	1.4 V Typical , 1.6 V max		
Duty Cycle   500	Output "Low" Voltage;	V <sub>OL</sub>		1.1 V Typical , 0.9 V min.		
Rise Time (Tr)/Fall Time (Tf) (20% V <sub>DD</sub> – 80% V <sub>DD</sub> )						
Current Consumption	Duty Cycle		50% ± 5%			
Current Consumption         100 MHz: 16 mA           V <sub>DD</sub> = +2.5V         250 MHz: 18 m/A           All values are typical and over operating temperatures.         1 GHz:24 mA           1.35 GHz: 26 mA         1.35 GHz: 26 mA           Current with Output Disabled Start-up Time         10 ms max.           Aging         ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years           OE Pad Input XOs: Pad 1 VCXOs: Pad 1 VCXOs: Pad 2         70% of V <sub>DD</sub> minimum or no connection to enable output. LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS		e (Tf)	0.2nS. typ. 0.4nS. max.			
Current Consumption         V <sub>DD</sub> = ±2.5V       250 MHz: 18 mA         All values are typical and over operating temperatures.       750 MHz: 21 mA         1 GHz: 24 mA       1.35 GHz: 26 mA         Current with Output Disabled       10 ms max.         Aging       ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years         OE Pad Input XOS: Pad 1       70% of V <sub>DD</sub> minimum or no connection to enable output. LVCMOS/LVTTL level.         30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level.         Output Enable Time       200 ns max.         Output Disable Time       50 ns max.         Phase Jitter, rms       1.0 pS typical; 1.5 pS max.         (12 KHz to 20 MHz)       1.0 pS typical; 1.5 pS max.         Phase Jitter, rms       1.0 pS typical; 1.5 pS (2002/95/EC) and WEEE (2002/96/EC)         ROHS Status       ROHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)         Storage Temp. Range       -55°C to 150°C         Humidity       85% RH, 85°C, 48 hours         Fine Leak / Gross Leak       MIL-STD-202F method 208E         Reflow       260°C for 10 sec. 2X.         Vibration       MIL-STD-202F method 214, 5sine wave         Resistance to Solvent       MIL-STD-202F method 215         Temperature Cycling </th <th>(2070 100 - 3070 100)</th> <th></th>	(2070 100 - 3070 100)					
V_DP = +2.5V	Current Consumption					
All values are typical and over operating temperatures.  750 MHz:22 mA 1 GHz:24 mA 1.35 GHz: 26 mA  Current with Output Disabled 16 mA typical  Start-up Time 10 ms max.  Aging ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years  Output Enable Function  OE Pad Input XOs: Pad 1 70% of V <sub>DD</sub> minimum or no connection to enable output. LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 30% of V <sub>DD</sub> max						
operating temperatures.  1 GHz:24 mA 1.35 GHz: 26 mA 1.35 GHz: 26 mA 1.0 ms max.  Aging 10 ms max.  Ag						
Current with Output Disabled Start-up Time 10 ms max.  Aging 42 ppm max, first year at 25°C; ±10 ppm max. over 10 years  Output Enable Function  OE Pad Input XOs: Pad 1 VCXOs: Pad 2 Output Enable Time Output Disable Time  Output Disable Time  Output Disable Time  Tom S (12 KHz to 20 MHz)  Phase Jitter, rms (1.875 MHz to 20 MHz)  ROHS Status  ROHS Status  ROHS Status  ROHS Compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)  Storage Temp. Range Humidity  S5°C, 48 hours Fine Leak / Gross Leak MIL-StD-202F method 208E Reflow  Resistance to Solvent MIL-STD-202F method 215 Temperature Cycling MIL-STD-202F, method 215 MIL-STD-202F, method 215 Temperature Cycling MIL-STD-202F, method 215						
Current with Output Disabled Start-up Time 10 ms max.  Aging ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years  Output Enable Function  OE Pad Input XOs: Pad 1 VCXOs: Pad 2 0utput Enable Time 200 ns max.  Output Enable Time 200 ns max.  Integrated Phase Jitter Phase Jitter, rms (12 KHz to 20 MHz) Phase Jitter, rms (1.875 MHz to 20 MHz)  ROHS Status  FROHS Status  ROHS Status  Frine Leak / Gross Leak MIL-StD-202F method 204, 35G, 50 to 2000 Hz Shock MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave Resistance to Solvent  MIL-STD-202F, method 2115 Temperature Cycling MIL-STD-202F, method 2015 MIL-STD-202F, method 2115 Temperature Cycling MIL-STD-2083, method 1010  Output Enable output. LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum or no connection to enable output. LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level.  100 ps tycind Phase Jitter 100 ps max.  100 ps typical; 1.5 pS max.  100 fs  Environmental Performance Specifications RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)  Storage Temp. Range 1-55°C to 150°C  Humidity 100 ps typical; 1.5 pS max.  100 fs  Environmental Performance Specifications RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)  Storage Temp. Range 1-55°C to 150°C  Humidity 100 ps typical; 1.5 pS max.  110 ps t	operating temperatures.					
Start-up Time 10 ms max.  Aging ±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years  Output Enable Function  70% of V <sub>pp</sub> minimum or no connection to enable output. LVCMOS/LVTTL level. 30% of V <sub>pp</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level. 200 ns max.  Output Enable Time 200 ns max.  Fine Suitter, rms (12 KHz to 20 MHz) 1.0 pS typical; 1.5 pS max.  Phase Jitter, rms (12 KHz to 20 MHz) 1.0 pS typical; 1.5 pS max.  ROHS Status 8 RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)  Storage Temp. Range -55°C to 150°C -55°C to 150°C Fine Leak / Gross Leak MIL-StD-202F method 208E  Reflow 260°C for 10 sec. 2X.  Vibration MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave Resistance to Solvent Temperature Cycling MIL-STD-883, method 1010	Comment with Output Disable 1					
Aging #2 ppm max. first year at 25°C; ±10 ppm max. over 10 years  Output Enable Function  OE Pad Input XOs: Pad 1 VCXOs: Pad 2  Output Enable Time						
OE Pad Input XOs: Pad 1 YCXOs: Pad 2 Output Enable Time Output Disable Time Output Disable Time Phase Jitter, rms (1.875 MHz to 20 MHz) ROHS Status ROHS Status Storage Temp. Range Humidity Fine Leak / Gross Leak Solderability Reflow Solderability Reflow Solderability Reflow Resistance to Solvent Temperature Cycling MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave Resistance to Solvent Temperature Cycling MIL-STD-202, method 215  Toutput Disable Output (high impedance). LVCMOS/LVTTL level. 200 ns max. Integrated Phase Jitter Phase Jitter, rms (1.875 MHz to 20 MHz) Integrated Phase Jitter I						
OE Pad Input XOs: Pad 1 VCXOs: Pad 2 Output Enable Time Output Disable Time Phase Jitter, rms (12 KHz to 20 MHz) Phase Jitter, rms (1.875 MHz to 20 MHz)  Storage Temp. Range Humidity Fine Leak / Gross Leak Solderability Fine Leak / Gross Leak Solderability Reflow Solderability Reflow Shock MIL-STD-202F method 2015 MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave Resistance to Solvent Temperature Cycling MIL-STD-202, method 215 Temperature Cycling MIL-STD-202, method 215 MIL-STD-202, method 215 Temperature Cycling MIL-STD-202, method 215 MIL-STD-202, method 215 MIL-STD-883, method 1010	Aging					
Output Disable Time 50 ns max.  Integrated Phase Jitter  Phase Jitter, rms (12 KHz to 20 MHz) 1.0 pS typical; 1.5 pS max.  Phase Jitter, rms (1.875 MHz to 20 MHz) < 100 fs  Calculate the second of t	XOs: Pad 1 VCXOs: Pad 2		70% of V <sub>DD</sub> minimum or no connection to enable output. LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level.			
Integrated Phase Jitter						
Phase Jitter, rms (12 KHz to 20 MHz)  Phase Jitter, rms (1.875 MHz to 20 MHz)  ROHS Status  ROHS Status  ROHS Compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)  Storage Temp. Range  Humidity  85% RH, 85°C, 48 hours  Fine Leak / Gross Leak  MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C  Solderability  MIL-STD-202F method 208E  Reflow  260°C for 10 sec. 2X.  Vibration  MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave  Resistance to Solvent  Temperature Cycling  MIL-STD-883, method 1010						
Comparison of the content of the c	Dhaga littar mas		integrated Phase Jitter			
County   C	(12 KHz to 20 MHz)	1.0 pS ty	oS typical; 1.5 pS max.			
ROHS Status  RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)  Storage Temp. Range -55°C to 150°C  Humidity 85% RH, 85°C, 48 hours  Fine Leak / Gross Leak MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C  Solderability MIL-STD-202F method 208E  Reflow 260°C for 10 sec. 2X.  Vibration MIL-STD-202F method 204, 35G, 50 to 2000 Hz  Shock MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave  Resistance to Solvent MIL-STD-202, method 215  Temperature Cycling MIL-STD-883, method 1010		< 100 fs	s			
Storage Temp. Range  -55°C to 150°C  Humidity  85% RH, 85°C, 48 hours  Fine Leak / Gross Leak  MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C  Solderability  MIL-STD-202F method 208E  Reflow  260°C for 10 sec. 2X.  Vibration  MIL-STD-202F method 204, 35G, 50 to 2000 Hz  Shock  MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave  Resistance to Solvent  Temperature Cycling  MIL-STD-883, method 1010						
Humidity85% RH, 85°C, 48 hoursFine Leak / Gross LeakMIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition CSolderabilityMIL-STD-202F method 208EReflow260°C for 10 sec. 2X.VibrationMIL-STD-202F method 204, 35G, 50 to 2000 HzShockMIL-STD-202F method 213B, test condi. E, 1000GG ½ sine waveResistance to SolventMIL-STD-202, method 215Temperature CyclingMIL-STD-883, method 1010	ROHS Status					
Humidity85% RH, 85°C, 48 hoursFine Leak / Gross LeakMIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition CSolderabilityMIL-STD-202F method 208EReflow260°C for 10 sec. 2X.VibrationMIL-STD-202F method 204, 35G, 50 to 2000 HzShockMIL-STD-202F method 213B, test condi. E, 1000GG ½ sine waveResistance to SolventMIL-STD-202, method 215Temperature CyclingMIL-STD-883, method 1010	Storage Temp. Range					
Fine Leak / Gross Leak  MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C  Solderability  MIL-STD-202F method 208E  Reflow  260°C for 10 sec. 2X.  Vibration  MIL-STD-202F method 204, 35G, 50 to 2000 Hz  Shock  MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave  Resistance to Solvent  MIL-STD-202, method 215  Temperature Cycling  MIL-STD-883, method 1010						
SolderabilityMIL-STD-202F method 208EReflow260°C for 10 sec. 2X.VibrationMIL-STD-202F method 204, 35G, 50 to 2000 HzShockMIL-STD-202F method 213B, test condi. E, 1000GG ½ sine waveResistance to SolventMIL-STD-202, method 215Temperature CyclingMIL-STD-883, method 1010						
Reflow260°C for 10 sec. 2X.VibrationMIL-STD-202F method 204, 35G, 50 to 2000 HzShockMIL-STD-202F method 213B, test condi. E, 1000GG ½ sine waveResistance to SolventMIL-STD-202, method 215Temperature CyclingMIL-STD-883, method 1010			· · · · · · · · · · · · · · · · · · ·			
VibrationMIL-STD-202F method 204, 35G, 50 to 2000 HzShockMIL-STD-202F method 213B, test condi. E, 1000GG ½ sine waveResistance to SolventMIL-STD-202, method 215Temperature CyclingMIL-STD-883, method 1010						
ShockMIL-STD-202F method 213B, test condi. E, 1000GG ½ sine waveResistance to SolventMIL-STD-202, method 215Temperature CyclingMIL-STD-883, method 1010						
Resistance to Solvent     MIL-STD-202, method 215       Temperature Cycling     MIL-STD-883, method 1010						
Temperature Cycling MIL-STD-883, method 1010						
<b>2000 v (per wile-310-003</b> , Hiethou 3013)						
	LOD Ratility					

### **Ordering Options:**

"x MHz " examples : 125.000000 MHz ; or 12.688375 MHz ; 1250.005600 MHz

### **Phase Noise Graphs**

### 212 MHz LVDS output



### LC!) !+!&') J!@I8GII A<n LVDS10 to 1450MHz Clock Oscillator

#### 1000 MHz LVDS output

