



### Features and Benefits

Frequency Range 10 MHz to 245 MHz  
 Output Frequency to six decimal places  
 Output Frequency Examples: 12.688375 MHz ; 125.345678 MHz  
 7 mm x 5.0 mm x 1.80 mm ceramic SMD 6-pad  
 ±50 ppm total stability over -40°C to 85°C  
 1 to 1.5 pico-second phase jitter ( 12KHz to 20 MHz )  
 LVCMOS output  
 3.3V supply

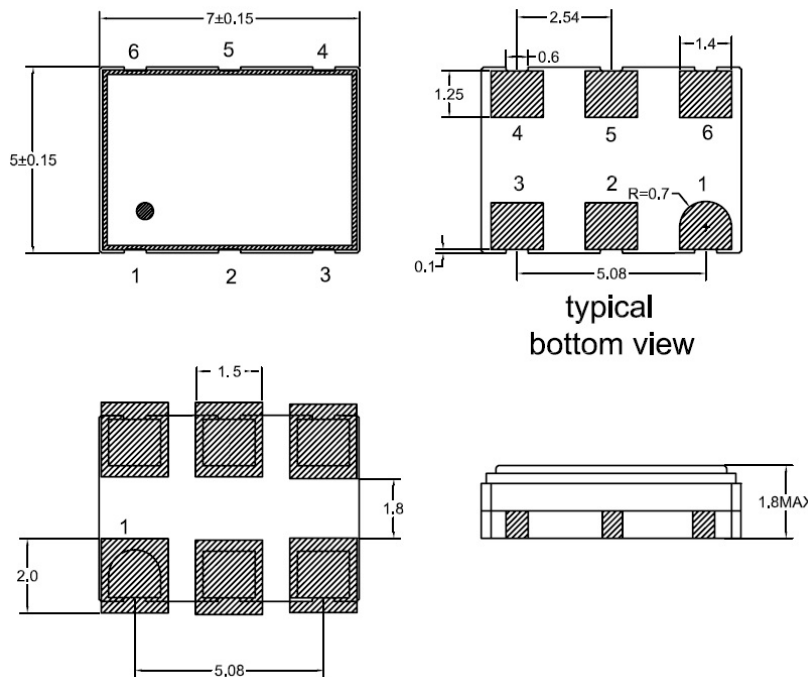
### Typical Applications

GbE Ethernet, SONET, Fibre channel, FPGA, and A/D clock reference devices

### Description

A new generation of low jitter / low power clock oscillators has been developed using the latest low noise integrated circuit topologies.

### Mechanical Drawing & Pin Connections



Product	XO	VCXO
Pad 1	High Enable	Voltage Control
Pad 2	No Connection	High Enable
Pad 3	Ground	
Pad 4	CMOS: Output LVPECL, LVDS: Differential Output	
Pad 5	CMOS: No connection LVPECL, LVDS: Complementary Output	
Pad 6	Supply voltage	



**Specifications**

<b>General Specifications: at Ta=+25°C,</b>		
<b>Output Logic Type</b>	LVCMOS	
<b>Frequency Range</b>	10 ~ 245 MHz	
<b>Load</b>	15pF	
<b>Power Supply Voltage (V<sub>DD</sub>)</b>	V <sub>DD</sub> = +3.3V D.C. ± 5%	
<b>Output “High” Voltage; V<sub>OH</sub></b>	Voltage (V <sub>OD</sub> )	90% V <sub>DD</sub>
<b>Output “Low” Voltage; V<sub>OL</sub></b>	Voltage (V <sub>OD</sub> )	10% V <sub>DD</sub>
<b>Frequency Stability</b>	±50 ppm over -40°C to 85°C Over all conditions	
<b>Duty Cycle</b>	50% ± 5%	
<b>Rise Time (Tr)/Fall Time (Tf)</b> (10% V <sub>DD</sub> – 90% V <sub>DD</sub> )	1.5 nS.typ. 3.0 nS. max.	
<b>Current Consumption</b> V <sub>DD</sub> = +3.3V All values are typical and over operating temperatures.	10 MHz: 17 mA	
	50 MHz: 20 mA	
	100 MHz: 24 mA	
	150 MHz: 28 mA	
	200 MHz: 33 mA	
	250 MHz: 37 mA	
<b>Current with Output Disabled</b>	16 mA typical	
<b>Start-up Time</b>	10 ms max.	
<b>Aging</b>	±2 ppm max. first year at 25°C; ±10 ppm max. over 10 years	
<b>Output Enable Function</b>		
<b>OE Pad Input</b> <b>XOs: Pad 1</b> <b>VCXOs: Pad 2</b>	70% of V <sub>DD</sub> minimum or no connection to enable output. LVCMOS/LVTTL level. 30% of V <sub>DD</sub> maximum to disable output (high impedance). LVCMOS/LVTTL level.	
<b>Output Enable Time</b>	200 ns max.	
<b>Output Disable Time</b>	50 ns max.	
<b>Integrated Phase Jitter</b>		
<b>Phase Jitter, rms</b> <b>(12 KHz to 20 MHz)</b>	1.0 pS typical; 1.5 pS max.	
<b>Phase Jitter, rms</b> <b>(1.875 MHz to 20 MHz)</b>	< 100 fs	
<b>Environmental Performance Specifications</b>		
<b>ROHS Status</b>	RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)	
<b>Storage Temp. Range</b>	-55°C to 150°C	
<b>Humidity</b>	85% RH, 85°C, 48 hours	
<b>Fine Leak / Gross Leak</b>	MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C	
<b>Solderability</b>	MIL-STD-202F method 208E	
<b>Reflow</b>	260°C for 10 sec. 2X.	
<b>Vibration</b>	MIL-STD-202F method 204, 35G, 50 to 2000 Hz	
<b>Shock</b>	MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave	
<b>Resistance to Solvent</b>	MIL-STD-202, method 215	
<b>Temperature Cycling</b>	MIL-STD-883, method 1010	
<b>ESD Rating</b>	>2000 V (per MIL-STD-883, method 3015)	



### Ordering Options:

“x MHz” examples : 125.000000 MHz ; or 12.688375 MHz ; 1250.005600 MHz

### Phase Noise Graphs

125 MHz CMOS output

