

Dynamic Engineers Inc.

2550 Gray Falls Dr., Suite#128, Houston, TX, 77077 TEL: 1-281-870-8822 EMAIL: Sales@DynamicEng.com

Features and Benefits

Frequency Range 10 MHz to 1450 MHz Output Frequency to six decimal places Output Frequency Examples: 12.688375 MHz ; 125.345678 MHz 7 mm x 5.0 mm x 1.80 mm ceramic SMD 6-pad ± 50 ppm total stability over -40°C to 85°C 1 to 1.5 pico-second phase jitter (12 KHz to 20 MHz) LVDS outputs 3.3V supply

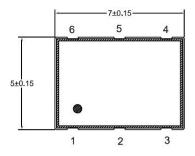
Typical Applications

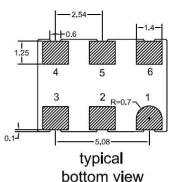
Gb Ethernet, SONET, Fibre channel, FPGA, and A/D clock reference devices

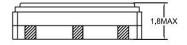
Description

A new generation of low jitter / low power clock oscillators has been developed using the latest low noise integrated circuit topologies.

Mechanical Drawing & Pin Connections







Product	ХО	VCXO	
Pad 1	High Enable	Voltage Control	
Pad 2	No Connection	High Enable	
Pad 3	Ground		
Pad 4	CMOS: Output LVPECL, LVDS: Differential Output		
Pad 5	CMOS: No connection LVPECL, LVDS: Complementary Output		
Pad 6	Supply voltage		



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Specifications

General Specifications: a	Ta=+25°C,			
Output Logic Type	LVDS			
Frequency Range	10 ~ 1450 MHz			
Load	Single - ended	Single - ended		
Power Supply Voltage (VD	1/ - 122/DC + 59/			
Output "High" Voltage; Vo	н Voltage (V _{OD})	1.4 V Typical , 1.6 V max		
Output "Low" Voltage; Vo	Voltage (V _{OD})	1.1 V Typical , 0.9 V max		
Frequency Stability	±50 ppm over -40°C to 85°C Over all conditions	±50 ppm over -40°C to 85°C Over all conditions		
Duty Cycle	50% ± 5%	50% ± 5%		
Rise Time (Tr)/Fall Time (T (20% V _{DD} – 80% V _{DD})	f) 0.2 nS typ. 0.4 nS max.	0.2 nS typ. 0.4 nS max.		
	100 MHz: 18 mA	100 MHz: 18 mA		
Current Consumption	250 MHz: 20 mA	250 MHz: 20 mA		
$V_{DD} = +3.3V$	500 MHz: 22 mA	500 MHz: 22 mA		
All values are typical and ov	er 750 MHz: 24 mA	750 MHz: 24 mA		
operating temperatures.	1 GHz: 26 mA	1 GHz: 26 mA		
		1.35 GHz: 28 mA		
Current with Output Disab	,1	16 mA typical		
Start-up Time		10 mS max.		
		C; ±10 ppm max. over 10 years		
	Output Enable F	unction		
OE Pad Input	70% of Vppminimum or no co	70% of V _{DD} minimum or no connection to enable output. LVCMOS/LVTTL level.		
XOs: Pad 1 VCXOs: Pad 2		30% of V _{DD} maximum to disable output (high impedance). LVCMOS/LVTTL level.		
Output Enable Time	200 nS mov	200 nS max.		
Output Disable Time		50 nS max.		
Output Disable Time		littor		
Phase Jitter, rms (12 KHz to 20 MHz)	0 pS typical; 1.5 pS max.	Integrated Phase Jitter S typical; 1.5 pS max.		
Phase Jitter, rms	100 fs	I		
(1.875 MHz to 20 MHz) <	Environmental Performan	co Specifications		
Environmental Performance Specifications RoHS Status RoHS compliant, Pb (lead) free in accordance with EU Directive 2002/95/EC 6/6				
ROHS Status	(2002/95/EC) and WEEE (20	(2002/95/EC) and WEEE (2002/96/EC)		
Storage Temp. Range		-55°C to 150°C		
Humidity		85% RH, 85°C, 48 hours		
Fine Leak / Gross Leak		MIL-Std-883, method 1014, condition A / MIL-Std-883, method 1014, condition C		
Solderability		MIL-STD-202F method 208E		
Reflow		260°C for 10 sec. 2X.		
Vibration		MIL-STD-202F method 204, 35G, 50 to 2000 Hz		
Shock		MIL-STD-202F method 213B, test condi. E, 1000GG ¹ / ₂ sine wave		
Resistance to Solvent	MIL-STD-202, method 215			
Temperature Cycling	,	MIL-STD-883, method 1010		
ESD Rating	>2000 V (per MIL-STD-883)	>2000 V (per MIL-STD-883, method 3015)		

Ordering Options:

"x MHz " examples : 125.000000 MHz ; or 12.688375 MHz ; 1250.005600 MHz

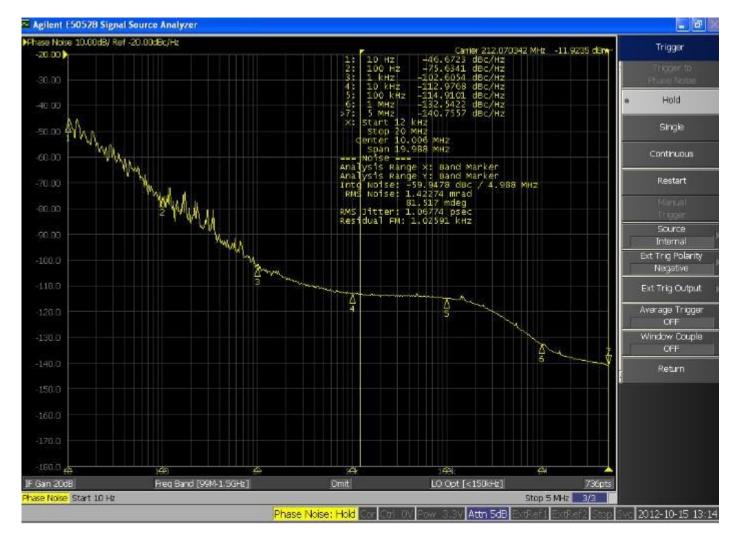
Dynamic Engineers reserves the right to make changes to the company datasheet(s) along with other information contained inside; such as data tables and araphs without notification to potential customers who may have earlier revisions in their possession.



XO-5-7-3.3V-LVDS-xMHz LVDS 10 to 1450 MHz Clock Oscillator

Phase Noise Graphs

212 MHz LVDS output



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1000 MHz LVDS output

