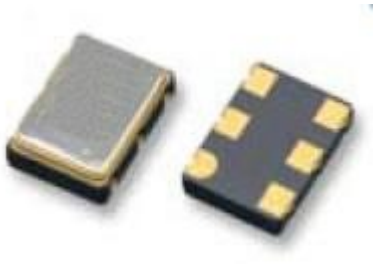
XO3001-100.000000-A
Very Low Jitter LVDS clock oscillator

Features

Standard 7x5x1.5mm ceramic 6-pad
Low phase jitter (0.7 ps max.)
Output frequency up to 320 MHz
Complementary Outputs
3.3V supply

Picture of Part



Typical Applications

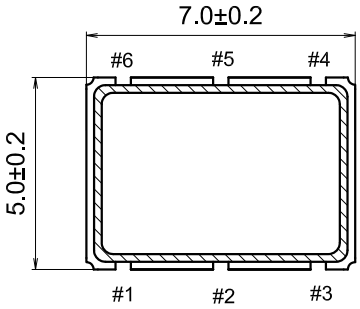
WLAN / WiMAX / WIFI
SONET / SDH / ATM
10 Gigabit Ethernet, Fiber Channel
xDSL

Description

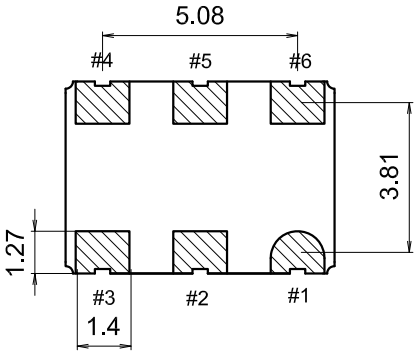
The XO3001 family offers ultra-low jitter PECL or LVDS outputs required of ever demanding data communications protocols around the world.

Mechanical Drawing and PIN Connections

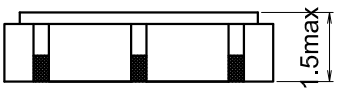
[TOP VIEW]



[BOTTOM VIEW]



[SIDE VIEW]



Pad	Function	
#1	NC	Tri-State
#2	Tri-State	NC
#3	GND	
#4	Output	
#5	Comp.Output	
#6	Vcc	

Specifications

XO Specification		Sym.	Condition	Value			Unit	Note
				Min.	Typ.	Max.		
Operational Frequency Range		f_0			100		MHz	
LVDS								
	H - level voltage	V_H				1.6	V	
	L - level voltage	V_L		0.9			V	
	Rise & Fall time		10% to 90%			1.0	ns	
							%	
Power supply								
Voltage		V_{CC}		3.150	3.300	3.450	V	
Current consumption		Icc				50	mA	
Tri-state Enable / Disable			Outputs Active	0.8 Vcc				The customer chooses either Pin 1 or Pin 2 for Tri-state
Pin 1 or Pin 2			Outputs NOT Active			0.2 Vcc		
Frequency stability								
vs. temperature			-40℃ to +85℃, ref 25℃	-20.0		+20.0	ppm	
							ppm	
OVERALL Stability :			Includes tolerance at 25C , aging	-30.0		+30.0	ppm	Variation with voltage, reflow shift
Integrated phase jitter 12KHz to 20 MHz			Fo <= 100 MHz			0.7	ps	
Aging	Per Year		Projected yearly aging after 30 days operation	-3.0		+3.0	ppm	
Environmental, mechanical conditions.								
Operating temperature range			**-40℃ to +85℃ maximum range available**					
Storage temperature range			**-55℃ to 125℃**					