Dynamic Engineers Inc.
2550 Gray Falls Dr., Suite#128, Houston, TX, 77077
TEL: 281-870-8822EMAIL:Sales@DynamicEngineers.com

XO7500R-100MHz-LV-A

5 X 7 mm SMD XO

Features and Benefits

10.0 MHz to 220 MHz operating frequency range for 3.3V supply
16 mA typical
Less than +/- 25 ppm over -40°C to +85°C
LVDS outputs
7.0 x 5.0 x 1.8 mm smd
3.3V supply voltage
200 fs typical integrated phase jitter (12KHz to 20 MHz)

Typical Applications

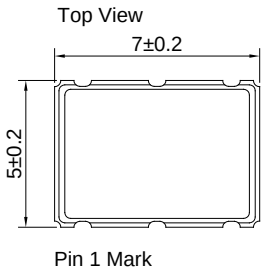
Telecom Networks
Data Communications

Description

The XO7500R series with LVDS outputs utilizes a fundamental crystal design that has no internal multiplication circuits to deliver the lowest possible phase jitter.

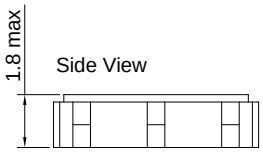
Mechanical Drawing & Pin Connections

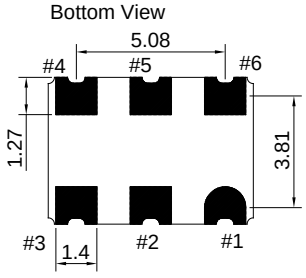
Drawing No: MD150071-1

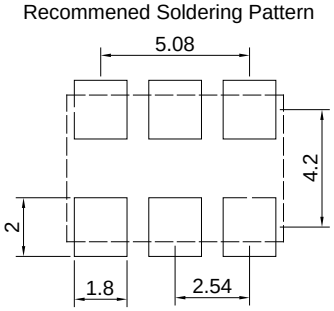


PIN	Function
PAD #1	Tri-State
PAD #2	N/C
PAD #3	GND
PAD #4	Output
PAD #5	Complimentary
PAD #6	Supply Voltage

Unit : mm







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Specifications

Oscillator Specification		Sym	Condition	Value			Unit	Note
				Min.	Typ.	Max.		
Nominal Frequency		F_{nom}			100		MHz	
Output Wave Form					LVDS			
Output Voltage Level "1"			RL=100 ohm	1.4		1.6	V	
Output Voltage Level "0"			RL=100 ohm	0.9		1.1	V	
Output Load			Between output and complimentary output		100		Ohm	
Duty Cycle				45	50	55	%	
Rise and Fall Times			20%<-->80% of the PECL wave form		0.2	0.4	nSec	
Start Time					5	10	mSec	
Output Voltage Swing			RL=100 ohm	250	350	450	mV	
Tri-State Function	No Connection		Differential LVDS and compliantary LVDS outputs					
	Disable		Both outputs are disabled (high impedance) when the Tri-state pad taken below 0.45*V_{CC} referenced to ground oscillator is always on. Only buffer stage is disabled. Disable current: 50uA max. (at 0V), Disable time: 10ns (Max.)					
	Enable		At disabled mode, both outputs are enabled when Tri-state pas is taken above 0.45*V_{CC} referenced to ground; Enable time: 10ns+ one period of the output frequency(max.)					
Power Supply								
Supply Voltage		V_{cc}		3.135	3.3	3.465	V	
Supply Current			15pF load		16	27	mA	
Frequency Stability								
Vs. Temperature			From -40°C to +85°C			+/-25	ppm	
Integrated Phase Jitter			12KHz to 20MHz		0.2	0.5	ps	
Aging			First year			+/-3	ppm	
			Per year thereafter			+/-2	ppm	
Phase Noise								
Phase Noise			@10Hz		-50		dBc/Hz	
			@100Hz		-80		dBc/Hz	
			@1KHz		-115		dBc/Hz	
			@10KHz		-135		dBc/Hz	
			@100KHz		-142		dBc/Hz	
			@1MHz		-147		dBc/Hz	
			@10MHz		-152		dBc/Hz	

Environmental Conditions		
Parameter	**Reference Std.**	**Test Condition**
Operating Temperature range	-40°C to +85°C	
Storage Temperature range	-55°C to +150°C	