### REVISIONS

<table>
<thead>
<tr>
<th>ZONE</th>
<th>REV</th>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>APPROVED</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td></td>
<td>SECTION 4 EXPANSIONS &amp; OTHER UPDATES</td>
<td>06/16/16</td>
<td>S.PALACIO</td>
</tr>
<tr>
<td>C1</td>
<td></td>
<td>EQUIPMENT/PROCEDURE UPDATE</td>
<td>07/05/16</td>
<td>S.PALACIO</td>
</tr>
<tr>
<td>C2</td>
<td></td>
<td>ENVIRONMENTAL SPECIFICATION UPDATE</td>
<td>07/18/16</td>
<td>S.PALACIO</td>
</tr>
<tr>
<td>D1</td>
<td></td>
<td>PERFORMANCE SPECIFICATION CHANGE</td>
<td>08/21/18</td>
<td>S.PALACIO</td>
</tr>
</tbody>
</table>

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**Planar Monolithics Industries, Inc.**

7311-F GROVE ROAD  
FREDERICK, MD 21704

**ACCEPTANCE TEST PROCEDURE**

MODEL: PLA-14D65G15G35G-20DB-SFF-250W  
PART NO: 27329630

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<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>PMI</th>
</tr>
</thead>
<tbody>
<tr>
<td>ORIGINAL RELEASE</td>
<td>05/13/16</td>
<td>M. BERRY</td>
</tr>
<tr>
<td>SECTION 4 EXPANSIONS &amp; OTHER UPDATES</td>
<td>06/16/16</td>
<td>M. BERRY</td>
</tr>
<tr>
<td>EQUIPMENT/PROCEDURE UPDATE</td>
<td>07/05/16</td>
<td>M. BERRY</td>
</tr>
<tr>
<td>ENVIRONMENTAL SPECIFICATION UPDATE</td>
<td>07/18/16</td>
<td>M. BERRY</td>
</tr>
<tr>
<td>PERFORMANCE SPECIFICATION CHANGE</td>
<td>8/21/18</td>
<td>SPU</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>ITEM NO</th>
<th>PARAMETER</th>
<th>PARAGRAPH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency Range</td>
<td>All Tests Performed Over 14.65 GHz - 15.35 GHz</td>
</tr>
<tr>
<td>2</td>
<td>Insertion Loss</td>
<td>4.1</td>
</tr>
<tr>
<td>3</td>
<td>Peak Power Handling</td>
<td>4.6</td>
</tr>
<tr>
<td>4</td>
<td>Pulse Width</td>
<td>4.7</td>
</tr>
<tr>
<td>5</td>
<td>Average Power</td>
<td>4.8</td>
</tr>
<tr>
<td>6</td>
<td>Attenuation</td>
<td>4.2</td>
</tr>
<tr>
<td>7</td>
<td>Attenuation Flatness</td>
<td>4.2</td>
</tr>
<tr>
<td>8</td>
<td>Attenuation Accuracy</td>
<td>4.2</td>
</tr>
<tr>
<td>9</td>
<td>P1dB Limiting Threshold</td>
<td>4.10</td>
</tr>
<tr>
<td>10</td>
<td>Flat Leakage</td>
<td>4.9</td>
</tr>
<tr>
<td>11</td>
<td>Switching Speed</td>
<td>4.11</td>
</tr>
<tr>
<td>12</td>
<td>Phase Matching</td>
<td>4.5</td>
</tr>
<tr>
<td>13</td>
<td>DC Consumption (+5 V)</td>
<td>4.4</td>
</tr>
<tr>
<td>14</td>
<td>DC Consumption (-15 V)</td>
<td>4.4</td>
</tr>
<tr>
<td>15</td>
<td>VSWR (Return Loss)</td>
<td>4.3</td>
</tr>
</tbody>
</table>
1.0 SCOPE

This procedure defines the tests required for the acceptance of a PMI Model PLA-14D65G15G35G-20DB-SFF-250W.

2.0 TEST EQUIPMENT

Test equipment shall be inspected for current calibration and serviceability. Test connectors shall be cleaned and inspected prior to test set connection. Coaxial test cables shall be inspected for proper impedance (i.e. 50 Ω coax for RF). **Test Equipment with equivalent or better specifications than the equipment defined in the table below may be substituted.** RF cables and adapters to be used as needed and proper calibration of test setup is required.

**TABLE OF EQUIPMENT**

<table>
<thead>
<tr>
<th>ITEM NO</th>
<th>ITEM</th>
<th>MANUFACTURER</th>
<th>MODEL NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PNA NETWORK ANALYZER</td>
<td>AGILENT</td>
<td>N5230A</td>
</tr>
<tr>
<td>2</td>
<td>E-CAL MODULE</td>
<td>AGILENT</td>
<td>N4692A</td>
</tr>
<tr>
<td>3</td>
<td>DC POWER SUPPLY (TRIPLE OUTPUT)</td>
<td>AGILENT</td>
<td>E3631A</td>
</tr>
<tr>
<td>4</td>
<td>SIGNAL GENERATOR</td>
<td>KEYSIGHT</td>
<td>E8257D</td>
</tr>
<tr>
<td>5</td>
<td>POWER METER</td>
<td>GIGATRONICS</td>
<td>8541C</td>
</tr>
<tr>
<td>6</td>
<td>POWER SENSOR (CW)</td>
<td>GIGATRONICS</td>
<td>80325A</td>
</tr>
<tr>
<td>7</td>
<td>POWER SENSOR (PEAK)</td>
<td>GIGATRONICS</td>
<td>80355A</td>
</tr>
<tr>
<td>8</td>
<td>POWER SENSOR (MODULATED)</td>
<td>GIGATRONICS</td>
<td>80425A</td>
</tr>
<tr>
<td>9</td>
<td>TWT AMPLIFIER</td>
<td>CPI</td>
<td>VZM6993J5 (Base 250W Model)</td>
</tr>
<tr>
<td>10</td>
<td>CIRCULATOR</td>
<td>PMI</td>
<td>RMCI.12-18Sf</td>
</tr>
<tr>
<td>11</td>
<td>50 Ω HIGH POWER LOAD</td>
<td>PMI</td>
<td>1431-2</td>
</tr>
<tr>
<td>12</td>
<td>WAVEFORM GENERATOR</td>
<td>AGILENT</td>
<td>33522A</td>
</tr>
<tr>
<td>13</td>
<td>OSCILLOSCOPE</td>
<td>AGILENT</td>
<td>MSOX3034A</td>
</tr>
<tr>
<td>14</td>
<td>DETECTOR (CRYSTAL OR DIODE)</td>
<td>PMI</td>
<td>DD-20-218-5PF-3-P-M-OPT0518</td>
</tr>
<tr>
<td>15</td>
<td>PERSONAL COMPUTER (PC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>DIGITAL MULTIMETER (DMM)</td>
<td>AGILENT</td>
<td>34401A</td>
</tr>
<tr>
<td>17</td>
<td>HIGH PASS FILTER</td>
<td>PMI</td>
<td>HP2G-1780-CD-SS</td>
</tr>
<tr>
<td>18</td>
<td>THERMAL PLATFORM (HOT/COLD PLATE)</td>
<td>ESS</td>
<td>T650</td>
</tr>
<tr>
<td>19</td>
<td>20 dB FIXED ATTN (200 W CW, 1 kW PEAK)</td>
<td>PMI</td>
<td>WA95-20-43</td>
</tr>
<tr>
<td>20</td>
<td>30 dB FIXED ATTN (200 W CW, 1 kW PEAK)</td>
<td>PMI</td>
<td>WA95-30-43</td>
</tr>
</tbody>
</table>
3.0 GENERAL REQUIREMENTS

Evidence supporting successful completion of in-process testing (ESS Testing) shall be verified prior to formal acceptance testing. The Device Under Test, or DUT, shall be closed prior to formal acceptance test to provide a tamper proof seal. At any point during testing a unit does not meet the required specifications, testing shall be manually or automatically (dependent on availability of automated setup) stopped.

3.1 TEST CONDITIONS

Unless specified otherwise, testing shall be performed at an ambient temperature of 24 °C ± 4°C and a relative humidity level not exceeding 90%. The DUT shall be conductively cooled in a manner that maintains the DUT case temperature within the specified ambient temperature window. PMI will test the DUT on a thermal platform (Item #18) to ensure temperature is regulated. The first unit will be characterized at the operating temperature extremes (-55 °C and +85 °C). Initial characterization to include all Section 4.0 test parameters listed below; the measured values may vary but will meet specifications over the operating temperature range.

3.2 TEST FAILURE

If test failure is indicated, the test program for the DUT shall be stopped by the technician. The cognizant engineering and quality representatives shall be notified. The engineering and quality representatives shall assess the failure to assign cause. A written course of action shall be developed by engineering and quality to determine the root cause of the failure.

4.0 TEST PROCEDURE

In order to verify that the design of the DUT achieves the desired specification requirements the device must be tested and the results recorded. The following procedures and techniques will be followed using the various layout diagrams illustrated below. All tests require DC power to be applied to the DUT.

4.1 INSERTION LOSS

a) Set PNA (Item #1) to 14.65 to 15.35 GHz Frequency Range at -10 dBm Input Power.
b) Calibrate the PNA Network Analyzer using the E-Cal Module (Item #2).
c) Connect cables to the DUT as seen in Figure 1 and display S-Parameters S12 and S21.
d) Set TTL logic to “0” = 0 dB Attenuation.
e) Measure and record Insertion Loss by setting Minimum and Maximum markers.

4.2 ATTENUATION, ATTENUATION FLATNESS, ATTENUATION ACCURACY

a) Set PNA (Item #1) to 14.65 to 15.35 GHz Frequency Range at -10 dBm Input Power.
b) Calibrate the PNA Network Analyzer using the E-Cal Module (Item #2).
c) Connect cables to the DUT as seen in Figure 1 and display S-Parameters S12 and S21.
d) Set TTL logic to “0” = 0 dB Attenuation.
e) Normalize the S12 and S21 to 0 dB.
f) Set TTL logic to “1” = 20 dB Attenuation.
g) Measure and record Attenuation, Attenuation Flatness and Attenuation Accuracy by setting Minimum and Maximum markers.
4.3 VSWR (RETURN LOSS)

a) Set PNA (Item #1) to 14.65 to 15.35 GHz Frequency Range at -10 dBm Input Power.
b) Calibrate the PNA Network Analyzer using the E-Cal Module (Item #2).
c) Connect cables to the DUT as seen in Figure 1 and display S-Parameters S11 and S22.
d) Set TTL logic to “0” = 0 dB Attenuation.
e) Measure and record VSWR/Return Loss using the PNA by setting a Maximum marker.
f) Set TTL logic to “1” = 20 dB Attenuation.
g) Measure and record VSWR/Return Loss using the PNA by setting a Maximum marker.

4.4 DC CURRENT CONSUMPTION

a) Connect cables to the DUT as seen in Figure 1.
b) Set TTL logic to “0” = 0 dB Attenuation.
c) Measure and record DC Current Consumption displayed on the power supply (Item #3) for both positive and negative voltages.
d) Set TTL logic to “1” = 20 dB Attenuation.
e) Measure and record DC Current Consumption displayed on the power supply for both positive and negative voltages.
f) Document the worst case positive and negative currents between steps 4.4.c and 4.4.e.

4.5 PHASE MATCHING

a) Set PNA (Item #1) to 14.65 to 15.35 GHz Frequency Range at -10 dBm Input Power.
b) Calibrate the PNA Network Analyzer using the E-Cal Module (Item #2).
c) Connect cables to the first unit as seen in Figure 1 and display S-Parameters S12 and S21.
d) Set TTL logic to “0” = 0 dB Attenuation.
e) Set S12 and S21 to measure Phase and normalize to 0°.
f) Store calibration setting as Phase at 0 dB Attenuation.
g) Set TTL logic to “1” = 20 dB Attenuation and normalize to 0° again.
h) Store calibration setting as Phase at 20 dB Attenuation.
i) Return TTL logic to “0” and recall Phase at 0 dB Attenuation calibration setting.
j) Record the Phase value for all units in the manufacturing lot in reference to the Normalized Unit. Ensure the largest difference in phase between all units is less than or equal to 15°.
k) Set TTL logic to “1” and recall Phase at 20 dB Attenuation calibration setting.
l) Record the Phase value for all units in the manufacturing lot in reference to the Normalized Unit. Ensure the largest difference in phase between all units is less than or equal to 15°.

4.6 PEAK POWER HANDLING

a) Set the signal generator (Item #4) with pulse modulation “ON” to match the pulse seen in Figure 2 by setting internal waveform generator pulse width and period settings.
b) Connect cables to DUT as seen in Figure 3 with the Peak Power Sensor (Item #7).
c) To account for loss throughout the system, the RF input power from the signal generator must be calibrated such that the level at the input of the DUT is +51 dBm (125 W).
   For -55°C and 85°C set up the input power level to +50 dBm (100 W).
d) Record the Peak Power Handling pass/fail criteria.
e) Perform this test at both 0 dB and 20 dB attenuation.
4.7 PULSE WIDTH

a) Set the signal generator (Item #4) to match the pulse seen in Figure 2 by setting internal waveform generator pulse width and period settings.
b) Connect cables to DUT as seen in Figure 4.
c) To account for loss throughout the system, the input power level from the signal generator must be calibrated such that the level at the input of the DUT is +51 dBm (125 W).
   For -55°C and 85°C set up the input power level to +50 dBm (100 W).
d) Record the Pulse Width found on the Oscilloscope (Item #13).
e) Perform this test at both 0 dB and 20 dB attenuation.

4.8 AVERAGE POWER

a) Set the signal generator (Item #4) with pulse modulation “ON” to match the pulse seen in Figure 2 by setting internal waveform generator pulse width and period settings.
b) Connect cables to DUT as seen in Figure 3 with the CW/Modulation Power Sensor (Item #6/Item #8).
c) To account for loss throughout the system, the RF input power from the signal generator must be calibrated such that the level at the input of the DUT is +51 dBm (125 W).
   For -55°C and 85°C set up the input power level to +50 dBm (100 W).
d) Record the Average Power at both 0 dB and 20 dB attenuation with both sensors.

4.9 FLAT LEAKAGE

a) Set the signal generator (Item #4) to match the pulse seen in Figure 2 by setting internal waveform generator pulse width and period settings.
b) Connect cables to DUT as seen in Figure 3.
c) Set TTL logic “0” = 0 dB Attenuation.
d) To account for loss throughout the system, the input power level from the signal generator must be calibrated such that the level at the input of the DUT is 0 dBm (1 mW).
e) Gradually increase the input power from 0 W to 125 W.
   For -55°C and 85°C increase input power from 0 W to 100 W
f) Record the Flat Leakage on the power meter (Item #5) using the CW sensor (Item #6).

4.10 P1dB LIMITING THRESHOLD

a) Connect cables to DUT as seen in Figure 5.
b) Set TTL logic to “0” = 0 dB Attenuation
c) Monitor the output power while gradually increasing the input power.
d) Graph the limiting curve found in PMI Test Data Sheet Document No: 27629633 and record the power in vs power out.
e) Locate the P1dB Limiting Threshold where the power in is reduced by 1 dB compared to the power out (insertion loss to be normalized to 0 dB) using the CW sensor (Item #6)
4.11 SWITCHING SPEED

a) Connect cables to DUT as seen in Figure 6 and calibrate for loss and delay in components.
b) Set the signal generator (Item #4) to a frequency range of 15 GHz at 20 dBm output power.
c) Set Oscilloscope to invert signal as the Crystal Detector or Diode Detector (Item #14) as they have a negative output.
d) Set Waveform Generator (Item #13) to +5 VDC Amplitude, Offset of +2.5 VDC, Pulsed at 1 MHz with a 50% Duty Cycle.
e) Measure and record Switching Speed from 50% TTL to 90%/10% RF.

5.0 TEST DIAGRAMS

FIGURE 1 – CONFIGURATION FOR TESTS 4.1 – 4.5
FIGURE 2 – PULSE DESCRIPTION, SETTINGS FOR SIGNAL GENERATOR

- 400 μs
- 40 μs
- 360 μs
FIGURE 3 – CONFIGURATION FOR TESTS 4.6, 4.8, 4.9

TWT AMPLIFIER

SIGNAL GENERATOR

CIRCULATOR

50 Ω

SENSOR GUIDE

<table>
<thead>
<tr>
<th>TEST</th>
<th>ITEM #</th>
</tr>
</thead>
<tbody>
<tr>
<td>CW</td>
<td>6</td>
</tr>
<tr>
<td>PEAK</td>
<td>7</td>
</tr>
<tr>
<td>MODULATED</td>
<td>8</td>
</tr>
</tbody>
</table>

DUT

30 dB ATTN (AS NEEDED)

POWER SENSOR (1 OF 3)

POWER SUPPLY

GND E2 +V -V

GND TTL +5V -15V

POWER METER
FIGURE 4 – CONFIGURATION FOR PULSE WIDTH TESTING

- **TWT AMPLIFIER**
- **SIGNAL GENERATOR**
- **CIRCULATOR**
- **OSCILLOSCOPE**
- **50 Ω**
- **DUT**
- **30 dB ATTN**
- **POWER SUPPLY**

Connections: TWT AMPLIFIER to SIGNAL GENERATOR, SIGNAL GENERATOR to OSCILLOSCOPE, OSCILLOSCOPE to DUT, DUT to POWER SUPPLY, POWER SUPPLY to TWT AMPLIFIER.
FIGURE 5 – CONFIGURATION FOR P1dB LIMITING THRESHOLD
FIGURE 6 – CONFIGURATION FOR SWITCHING SPEED

SIGNAL GENERATOR

OSCILLOSCOPE

CH1

CH2

DUT

IN

GND E2

TTL

+V

-V

OUT

HIGH PASS FILTER

IN

DETECTOR

OUT

POWER SUPPLY

GND

TTL

+5V

-15V

WAVE FORM GENERATOR
# 6.0 TEST DATA SHEET

## SUMMARY TEST DATA ON PLA-14D65G15G35G-20DB-SFF-250W

<table>
<thead>
<tr>
<th>Test Item No.</th>
<th>Parameters</th>
<th>Specified Value</th>
<th>Test Measurement</th>
<th>Test Result</th>
<th>QA/QC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency Range</td>
<td>14.65 To 15.35 GHz</td>
<td>14.65 To 15.35 GHz</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Insertion Loss</td>
<td>3.59 dB Max&lt;sup&gt;1&lt;/sup&gt;</td>
<td>dB</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Power Handling</td>
<td>Low Temp (-55 °C) 100 W Max&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Pass/Fail</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Room Temp (+25 °C) 125 W Max&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Pass/Fail</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Temp (+85 °C) 100 W Max&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Pass/Fail</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Pulse Width</td>
<td>40 µs Typ&lt;sup&gt;2&lt;/sup&gt;</td>
<td>µs</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Average Power</td>
<td>Low Temp (-55 °C) 10 W Max&lt;sup&gt;2&lt;/sup&gt;</td>
<td>W</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Room Temp (+25 °C) 12.5 W Max&lt;sup&gt;2&lt;/sup&gt;</td>
<td>W</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Temp (+85 °C) 10 W Max&lt;sup&gt;2&lt;/sup&gt;</td>
<td>W</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Attenuation</td>
<td>Logic TTL &quot;0&quot; = 0 dB</td>
<td>Pass/Fail</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Logic TTL &quot;1&quot; = 20 dB</td>
<td>Pass/Fail</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Attenuation Flatness</td>
<td>±1 dB Max</td>
<td>dB</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Attenuation Accuracy</td>
<td>±1 dB Max</td>
<td>dB</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>P1dB Limiting Threshold</td>
<td>+5 dBm Min</td>
<td>dBm</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Flat Leakage</td>
<td>+20 dBm Max @ 0 dB Attenuation And 100 W Max</td>
<td>dBm</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+20 dBm Max @ 0 dB Attenuation And 125 W Max</td>
<td>dBm</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+20 dBm Max @ 0 dB Attenuation And 100 W Max</td>
<td>dBm</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Switching Speed</td>
<td>90 ns, 50% TTL To 10% RF Max</td>
<td>ns</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>90 ns, 50% TTL To 90% RF Max</td>
<td>ns</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Phase Matching</td>
<td>15° Max Between Units @ 0 dB</td>
<td>ns</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15° Max Between Units @ 20 dB</td>
<td>ns</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>DC Consumption</td>
<td>+5 V @ 150 mA Max</td>
<td>mA</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>DC Consumption</td>
<td>-15 V @ 150 mA Max</td>
<td>mA</td>
<td>Pass/Fail</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>VSWR</td>
<td>2.0:1 Max @ 10 dBm Input</td>
<td>:1</td>
<td>Pass/Fail</td>
<td></td>
</tr>
</tbody>
</table>

1. @ -10 dBm Input & 0 dB Attenuation
2. @ 0 dB & 20 dB Attenuation with 10% Duty Cycle

QA/QC Approval: _____________________________ Date: _____________________________

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7311-F Grove Road Frederick, MD 21704 USA Phone: (301)662-5019 Fax: (301)662-1731
Email: sales@pmi-rf.com
SUMMARY TEST DATA
ON
PLA-14D65G15G35G-20DB-SFF-250W

S-Parameter Plots
Attenuation, Attenuation Flatness, Attenuation Accuracy, Return Loss
(IN/OUT) & Phase Matching

Page 3 of 4
SUMMARY TEST DATA
ON
PLA-14D65G15G35G-20DB-SFF-250W

LIMITER RESPONSE WITH FREQUENCY

OUTPUT POWER (dBm)

RF INPUT POWER (dBm)

14.65 GHz
15.0 GHz
15.35 GHz

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7311-F Grove Road Frederick, MD 21704 USA Phone: (301)662-5019 Fax: (301)662-1731
Email: sales@pmi-rf.com
7.0 PRODUCT FEATURE

DESCRIPTION
PMI MODEL: PLA-14D56G015G35G-20DB-SFF-250W IS AN INTEGRATED LIMITER AND ATTENUATOR THAT OPERATES AT 14.65 TO 15.35 GHz. THE INSERTION LOSS IS 3.59 dB MAXIMUM AND OFFERS 20 db OF ATTENUATION CONTROL VIA A SINGLE LINE TTL SIGNAL. THIS MODEL IS DESIGNED TO HANDLE 125 WATTS PEAK HAVING A PULSE WIDTH OF 40 us AND AN AVERAGE POWER OF 12.5 WATTS.

SPECIFICATIONS
- FREQUENCY RANGE: 14.65 TO 15.35 GHz
- INSERTION LOSS: 3.59 dB MAX
- PEAK POWER HANDLING
  - LOW TEMP (-55 °C): 100 W MAX
  - ROOM TEMP (+25 °C): 125 W MAX
  - HIGH TEMP (+85 °C): 100 W MAX
- PULSE WIDTH: 40 μs TYP
- AVERAGE POWER
  - LOW TEMP (-55 °C): 10 W MAX
  - ROOM TEMP (+25 °C): 12.5 W MAX
  - HIGH TEMP (+85 °C): 10 W MAX
- ATTENUATION
  - LOGIC TTL "0" - 0 dB ATTENUATION
  - LOGIC TTL "1" - 20 dB ATTENUATION
- ATTENUATION FLATNESS: ±1 dB MAX
- ATTENUATION ACCURACY: ±1 dB MAX
- PdB LIMITING THRESHOLD: -5 dBm MIN

1. @ -10 dBm INPUT AND 0 dB ATTENUATION
2. @ 0 dB AND 20 dB ATTENUATION @ 10% DUTY CYCLE

ENVIRONMENTAL RATINGS
- TEMPERATURE: -55 °C TO +85 °C (OPERATING)
- HUMIDITY: MIL-STD-810F
- SHOCK: MIL-STD-810F, METHOD 516.5, PROCEDURE 1
- VIBRATION: MIL-STD-810F, METHOD 514.5
- ALTITUDE: MIL-STD-810F, METHOD 622.2, PROCEDURE 3
- TEMPERATURE CYCLE: MIL-STD-810F, METHOD 601.4, 602.4

NOTE: THE ABOVE SPECIFICATIONS ARE SUBJECT TO CHANGE OR REVISION.