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A Field-Effect Transistor That Avoids Pinch-Off

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Greater efficiency and output power are proposed by providing a uniform depletion region along the channel to avoid pinch-off. A bias network to achieve this condition is described for a field-effect transistor (FET) with a segmented gate.

The efficiency of a FET is degraded when its drain voltage is greater than V_{Dsat}, the voltage at which pinch-off first occurs. Under this condition, the FET is in saturation, where the drain current is not a function of the drain voltage and is only a function of the gate voltage. To understand the degradation of efficiency, consider the behavior of a FET in saturation. When the drain voltage of a JFET, for instance, is equal to V_{Dsat}, pinch-off occurs exactly at the drain of the transistor (see ***Figure 1a***).[1] If the drain voltage is increased by ΔV, the point at which pinch-off occurs moves toward the source a distance ΔL (see ***Figure 1b***). Over the length, ΔL, the channel is completely depleted, and the resistance is quite large. Voltage, ΔV, is dropped across this depleted region and, due to its high resistivity, ΔL is very small. For ΔL << L, which represents the usual case, depletion from the source to the pinch-off point is essentially identical in shape, and the channel has approximately the same resistance from the source to the point where pinch-off occurs. The drain current, which is equal to V_{Dsat} divided by this resistance, hardly changes. This explains why the value of the drain current is nearly constant for drain voltages greater than V_{Dsat}. Over the length, ΔL, the resistance is quite large and the power dissipated in this resistance is equal to the product of the saturated current and ΔV. The voltage, ΔV, does not contribute to output power and simply degrades efficiency.

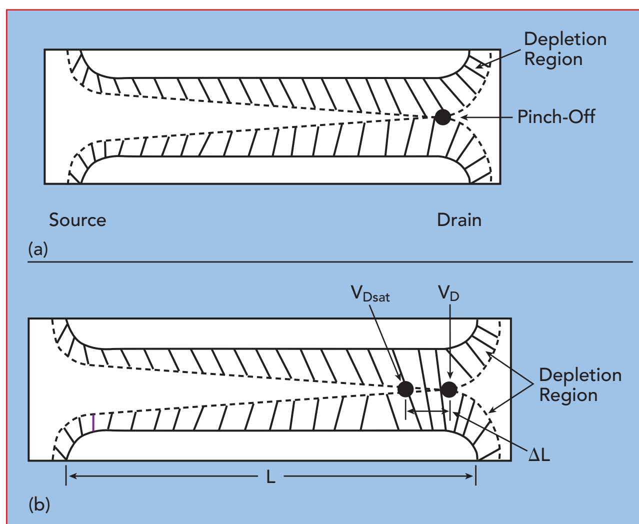

Fig. 1 Channel of a JFET with the drain voltage equal to the pinch-off voltage (a) and the drain voltage exceeding the pinch-off voltage (b).

Therefore, for high efficiency, pinch-off must be avoided, and the depletion region must be minimized. Ideally, for converting DC power to RF power, the channel should not be depleted for one-half the cycle and should be completely cut off for the other half. With an optimum load, this should yield maximum DC-to-RF efficiency. To accomplish this, a new FET has been proposed[2].

THE "GRAYZEL" JFET

Figure 2 shows a simplified schematic of a typical JFET with a drain-to-source DC voltage of 7 V. Points along the channel have voltage values of 0, 1, 2, 3, 4, 5, 6 and 7 V, as shown in the figure. The junction is progressively back-biased by these potentials, causing greater depletion at the drain than at the source. ***Figure 3*** shows a simplified schematic of the proposed device. The P+ region is divided into N sections that are insulated from one another, forming N, p-n junctions. As an illustrative example, in Fig-

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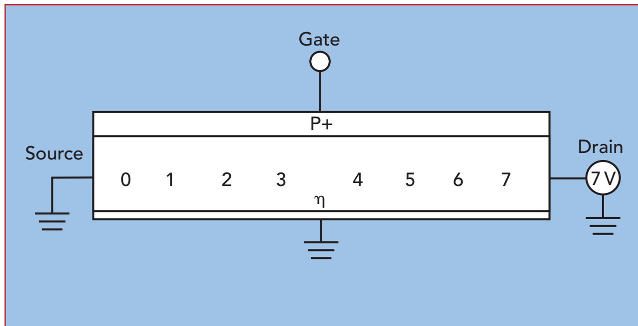

Fig. 2 Voltage drop across the channel of a typical JFET, with V_D = 7 V.

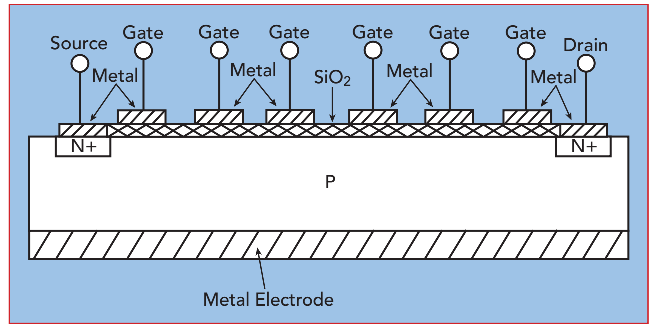

Fig. 4 Simplified cross-section of the proposed MOSFET.

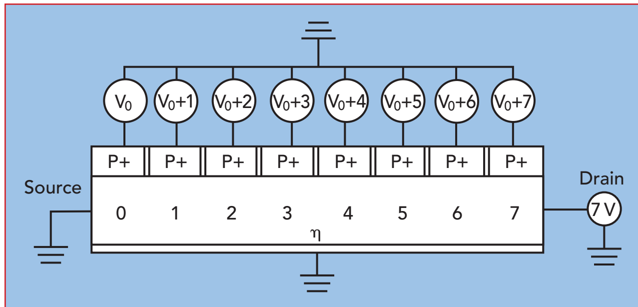

Fig. 3 Proposed JFET where the p-n junctions are individually biased and each junction is reverse biased at V_0.

to ground separately as shown in the figure; the first is biased at V_0 and the eighth at V_0 + 7 V. With a drain voltage of 7 V, all of the p-n junctions have the same DC voltage, V_0, across their junctions and hence, to a good approximation, the depletion region is uniform along the channel.

Dividing the gate into multiple sections is applicable to all types of FETs. ***Figure 4*** shows an example of a MOSFET with the gate divided into N = 6 sections. ***Figure 5*** shows a bias network with a drain voltage of 5V, biased such that each CMOS capacitor has a voltage of 5 V across it. The bias network consists of a 10 V DC voltage source and six resistors, which can be etched onto the chip.

ANALYSIS

Consider a case where the odd harmonics are short circuited and the even harmonics are open circuited by the load admittance Y(ω) and where, for half of the cycle, the FET is cut off and, for the other half, the depletion region in the channel is minimum width. The conductance is thus a square wave varying between 0 and G_0, where G_0 is the conductance when the depletion region in the channel is the minimum width. Let $\theta = 2\pi ft = \omega t$, where f is the fundamental frequency of the square wave. The Fourier series of the square wave is given by

$$G(t) = 0.5G_0 + g(t) \tag{1a}$$

where

$$g(t) = (2G_0/\pi)\left(\cos\theta - \cos(3\theta)/3 + \cos(5\theta)/5 - \cos(7\theta)/7 + \ldots\right.$$

$$= (2G_0/\pi)\sum_{k=1}^{\infty}(-1)^{k-1}\cos\left[(2k-1)\theta\right]/(2k-1)\right] \tag{1b}$$

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The FET is terminated in an admittance Y(ω), which at the fundamental frequency has a value GL. The value of Y(ω) = 0 at the even harmonics of the fundamental frequency and infinite at the odd harmonics. The drain voltage, therefore, has only even harmonics, and the drain current has only odd harmonics. The drain voltage, $V_D(t)$, has the form

$$V_D(t) = V_0 + v(t) \quad (2)$$

where

$$v(t) = V_1 \cos(\theta) + \sum_{k=1}^{\infty} V_{2k} \cos(2k\theta) \quad (3)$$

The bias voltage V_0 in Equation 2 is the same for all of the segments when the proposed FET is biased as described. There is, however, a variation of the depletion region along the channel, due to v(t). This variation is small and, therefore, it is neglected in this analysis.

Equation 3 represents the voltage v(t) for the following reason. The value of the conductance of the channel is equal to G_0 when −90 degrees < θ < +90 degrees, and the channel is cutoff during the remainder of the cycle; therefore, current flows only when −90 degrees < θ < +90 degrees. Since the current is equal to $V_D(t)G(t)$, $V_D(t)$ has its maximum value centered at θ = 0 degrees and is the sum of cosines.

Fig. 5 MOSFET bias network.

Fig. 6 FET amplifier.

Fig. 7 FET amplifier equivalent circuit.

The proposed segmented-gate amplifier shown in ***Figure 6*** is analyzed with the aid of the circuit in ***Figure 7***. Voltage v(t) appears across the RF choke and across the load Y(ω), which is in series with blocking capacitor C. V_0 + v(t) appears across the nonlinear conductance G(t). The choke, which is in series with the DC battery, has voltage v(t) across it but negligible RF current flowing through it. Drain current $I_D(t) = I_0$ + i(t) is equal to the product $G(t)V_D(t)$. i(t) flows in a loop through the termination Y(ω). DC voltage, V_0, appears across the blocking capacitor C. The drain current is given by

$$I_D(t) = V_D(t)G(t) = [V_0 + v(t)][0.5G_0 + g(t)] = 0.5V_0G_0 + V_0g(t) + 0.5G_0v(t) + v(t)g(t) \quad (4)$$

Equations 2, 3 and 4 yield the terms in Equation 4

$$V_0g(t) = (2V_0G_0/\pi)\left(\sum_{k=1}^{\infty}(-1)^{k-1}\cos[(2k-1)\theta]/[2k-1]\right) \quad (4a)$$

and

$$0.5G_0v(t) = 0.5G_0\left[V_1\cos(\theta) + \sum_{k=1}^{\infty} V_{2k}\cos(2k\theta)\right]$$

$$v(t)g(t) = (2G_0/\pi)\left[V_1\cos(\theta) + \sum_{k=1}^{\infty} V_{2k}\cos(2k\theta)\right]\sum_{j=1}^{\infty}(-1)^{j-1}\cos[(2j-1)\theta]/(2j-1)$$

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The drain current is the sum of a DC term, odd harmonics and even harmonics

$$I_d(t) = I_0 + \sum^{\infty}{}_{k=1}(I_{2k-1}) \cos(2k-1)\theta + \sum^{\infty}{}_{k=1} I_{2k} \cos(2k\theta) \quad (5)$$

Using the identity cos(x)cos(y) = 0.5[cos(x + y) + cos(x − y)] in Equation 4a, the even harmonics can be written as

$$I_{2k} = G_0 \left[0.5V_{2k} - (2V_1/\pi)(-1)^k / \left(4k^2 - 1\right)\right] \quad (6)$$

Since the current at the even harmonics is zero, it is possible to solve for voltage V_{2k} by setting current $I_{2k} = 0$ in Equation 6, yielding

$$V_{2k} = (4/\pi)(V_1)(-1)^k / \left(4k^2 - 1\right) \quad (7)$$

Collecting the terms in cos(θ) in Equation 4, the value of the current at the fundamental frequency, I_1, is

$$I_1 = G_0 \left[2V_0/\pi + 0.5V_1 - (2/\pi) \cdot \sum^{\infty}{}_{k=1}(-1)^k V_{2k} / \left(4k^2 - 1\right)\right] \quad (8)$$

Substituting Equation 7 into Equation 8 yields

$$I_1 = G_0\left\{2V_0/\pi + V_1\left[0.5 - \left(8/\pi^2\right)\sum^{\infty}{}_{k=1} 1/\left(4k^2 - 1\right)^2\right]\right\} \quad (9)$$

The term $[0.5 - (8/\pi^2) \Sigma^{\infty}{}_{k=1} 1/(4k^2 - 1)^2]$ converges in the limit to $(2/\pi)^2$ as k approaches infinity. (This limit was first estimated and then verified by a computer program.) Substituting $(2/\pi)^2$ for $[0.5 - (8/\pi^2) \Sigma^{\infty}{}_{k=1} 1/(4k^2 - 1)^2]$ in Equation 9 yields

$$I_1 = G_0\left[2V_0/\pi + (2/\pi)^2 V_1\right] \quad (10)$$

At the fundamental frequency $Y(\omega) = G_L$ and $I_1 = -(G_L)(V_1)$. Equating I_1 as given by Equation 10 to $-(G_L)(V_1)$, yields

$$2G_0V_0/\pi + G_0V_1(2/\pi)^2 = -G_LV_1 = -XG_0V_1 \quad (11)$$

where $X = G_L / G_0 = 1 / (G_0R_L)$.

Solving Equation 11 for V_1 yields

$$V_1 = -(2/\pi)V_0 / \left(X + (2/\pi)^2\right) \quad (12)$$

The DC current I_0 is found from Equation 4 to have two terms. The first term is $0.5(G_0)(V_0)$ and the second DC term results from the product $(2G_0/\pi)\cos(V_1\cos\theta)$.

$$I_0 = 0.5G_0V_0 + G_0V_1/\pi = 0.5G_0V_0\left[1 + (2/\pi)/(V_1/V_0)\right] \quad (13)$$

Substituting Equation 12 into Equation 13 yields

$$I_0 = 0.5G_0V_0X / \left(X + (2/\pi)^2\right) \quad (14)$$

The DC power is

$$P_0 = I_0V_0 = 0.5G_0V_0^2X / \left(X + (2/\pi)^2\right) \quad (15)$$

The output power at the fundamental frequency P_1 is

$$P_1 = 0.5G_LV_1^2 = 0.5G_L \cdot \left[(2/\pi)V_0 / \left(X + (2/\pi)^2\right)\right]^2 \quad (16)$$

The efficiency, EFF, is then

$$EFF = P_1/P_0 = (2/\pi)^2 / \left[X + (2/\pi)^2\right] \quad (17)$$

Figure 8 shows a plot of efficiency as a function of $X = G_L / G_0$.

This special case where the amplifier is terminated in an open circuit for the even harmonics and a short circuit for the odd harmonics gives good efficiency; however, it is not necessarily the optimum termination. An analysis similar to the one performed above, for the case where the amplifier is terminated in an open circuit for the odd harmonics and a short circuit for the even harmonics gives a

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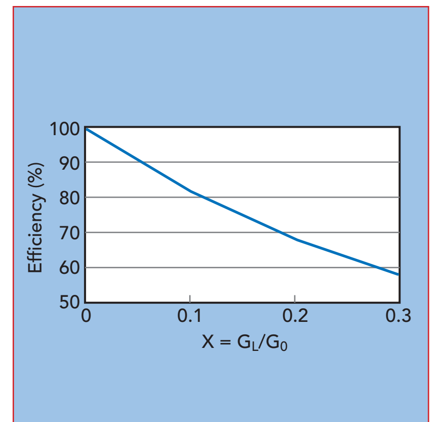

Fig. 8 Amplifier efficiency vs. X.

poorer result. An optimization is warranted to determine the best termination.

SUMMARY

A FET has greater efficiency and output power if pinch-off is avoided and the depletion region is made uniform along the channel. A bias network is presented for achieving this condition for a FET whose gate is segmented. Efficiency and output power are derived for the case where odd harmonics are short circuited and even harmonics are open circuited and where for half of the cycle the FET is off, while for the other half of the cycle the depletion region is minimum width.■

ACKNOWLEDGMENT

The author wishes to acknowledge the support provided by Ashok Gorwara, CEO, and the staff of Planar Monolithics Industries Inc.

Editor's Note

In a future issue of *Microwave Journal*, we hope to publish measured data confirming this theoretical FET structure.

References

1. R. F. Pierret, "Field Effect Devices: Modular Series on Solid State Devices," *Addison-Wesley Publishing Company*, 1983, pp. 5–15.
2. "Field Effect Transistor Which Can Be Biased to Achieve a Uniform Depletion Region," U.S. Patent 10,084,054.

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