A New Field Effect Transistor Which Avoids Pinchoff

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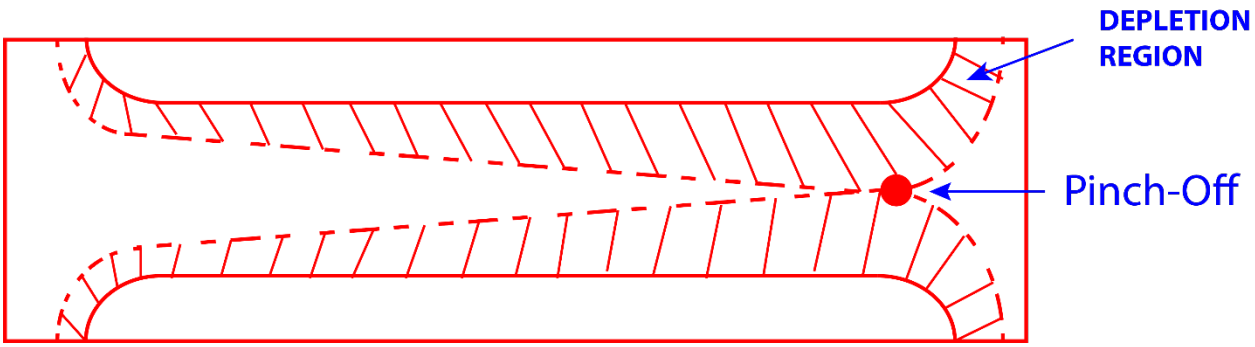
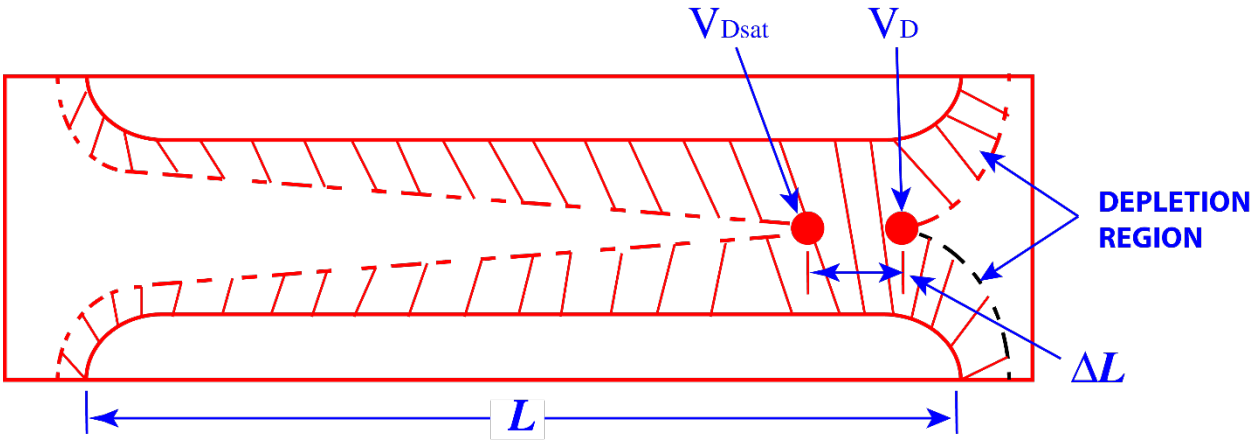
Abstract – We show that by segmenting the gate of an FET and applying appropriate biasing, pinchoff can be avoided and in the channel of the FET, a uniform depletion region can be achieved. This maximizes the efficiency and output power. Examples of biasing networks that achieve a uniform depletion region are presented. The efficiency and power output for this new FET is presented for the special case where the odd harmonics are short circuited, and the even harmonics are open circuited and where for half of the cycle the "Grayzel FET" is cutoff and for the other half of the cycle the depletion region in the channel is of minimal width.

1: Introduction

Let us examine the behavior of the FET in saturation. When the drain voltage of a JFET for instance, is exactly equal to the saturated drain voltage V_{dsat}, the conditions are those of Figure 1(a) [1], where pinchoff occurs exactly at the drain of the transistor. If the drain voltage is increased by ΔV, the point at which pinchoff occurs moves towards the source a distance of ΔL, as shown in Figure 1(b). Over the length ΔL, the channel is completely depleted and the resistance is quite large. Voltage ΔV is dropped across this depleted region and due to the high resistivity in the depleted region, ΔL is very small. For $\Delta L << L$, which represents the usual case, the depletion from source to pinchoff point will be essentially identical in shape and the channel will have essentially the same resistance from the source to the point where pinchoff now occurs. The drain current, which is equal to V_{dsat} divided by this resistance, hardly changes. This explains why the value of the drain current is nearly constant for drain voltages greater than V_{dsat}. Over the length ΔL the resistance is quite large and the power dissipated in this resistance is equal to the product of the saturated current and ΔV. The voltage ΔV does not contribute to the output power and simply degrades the efficiency. It is therefore clear that, for high efficiency pinchoff needs to be avoided and the depletion region must be minimized. Ideally, for converting DC power to RF power, the channel should have no depletion at all for one-half the cycle and should be completely cut-off for the other one-half cycle. With the optimum load, this should yield the maximum DC-to-RF efficiency. To accomplish this, a new (patent pending) FET is proposed, which will be referred to as the "Grayzel FET."



1a.



1b.

Figure 1. The diagrams show the channel of a JFET under different conditions: (a) when the drain voltage equals the pinchoff voltage and (b) when the drain voltage exceeds the pinchoff voltage.

2: The "Grayzel JFET"

Figure 2 shows a simplified schematic of a JFET with a drain voltage of seven volts DC. Points along the channel have values of potential of 0, 1, 2, 3, 4, 5, 6, and 7 V as shown in the figure. The junction is progressively back-biased by these potentials, causing greater depletion at the drain than at the source. Figure 3 shows a simplified schematic diagram of the "Grayzel JFET." The p+ region is divided into N sections that are insulated from one another, forming N, p-n junctions. (In Figure 3, N is equal to 8 as an illustrative example.) Each p-n junction is biased to ground separately as shown in Figure 3; the first at V_0 and the eighth at $V_0 + 7$. With a drain voltage of seven volts, all of the p-n junctions will have the same DC voltage V_0 across their junctions and hence, to a good approximation the depletion region will be uniform along the channel.

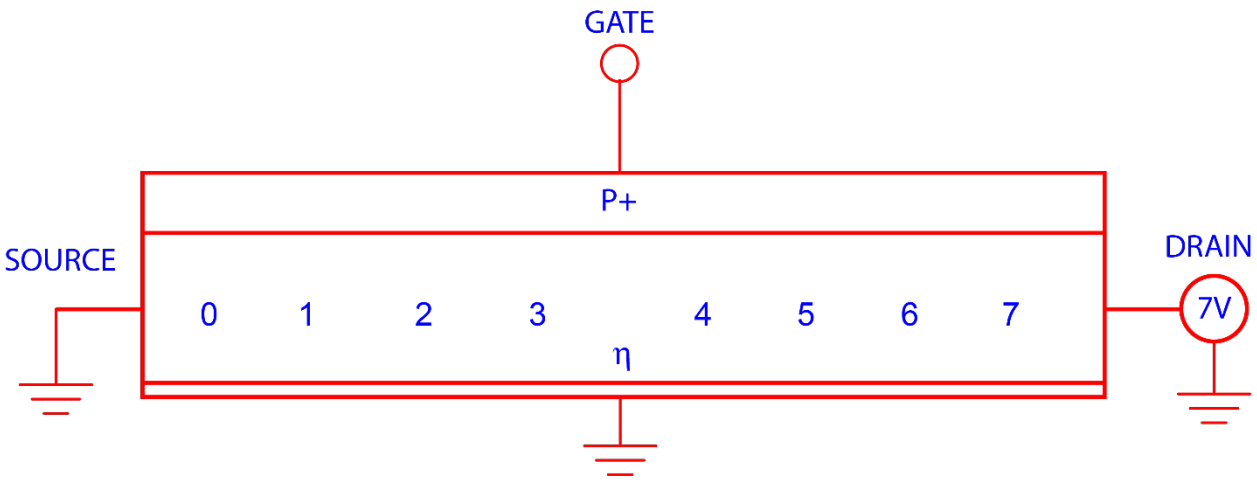


Figure 2. Voltage Drop Down the Channel of a JFET for a Drain Voltage of 7 Volts.

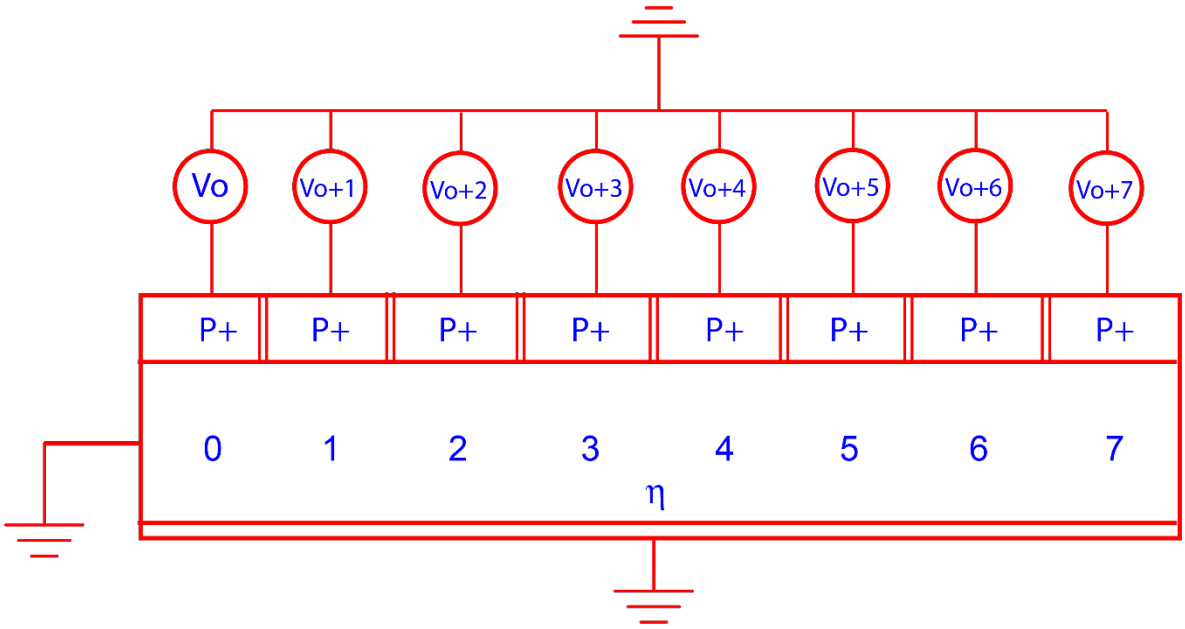


Figure 3. A "Grayzel JFET" where the p-n junctions are individually biased such that each p-n junction is reverse biased at voltage V_0.

Dividing the gate into multiple sections is applicable to all types of FETs. Figure 4 shows an example of the (patent pending) "Grayzel MOSFET" with the gate divided into N sections, with N = 6.

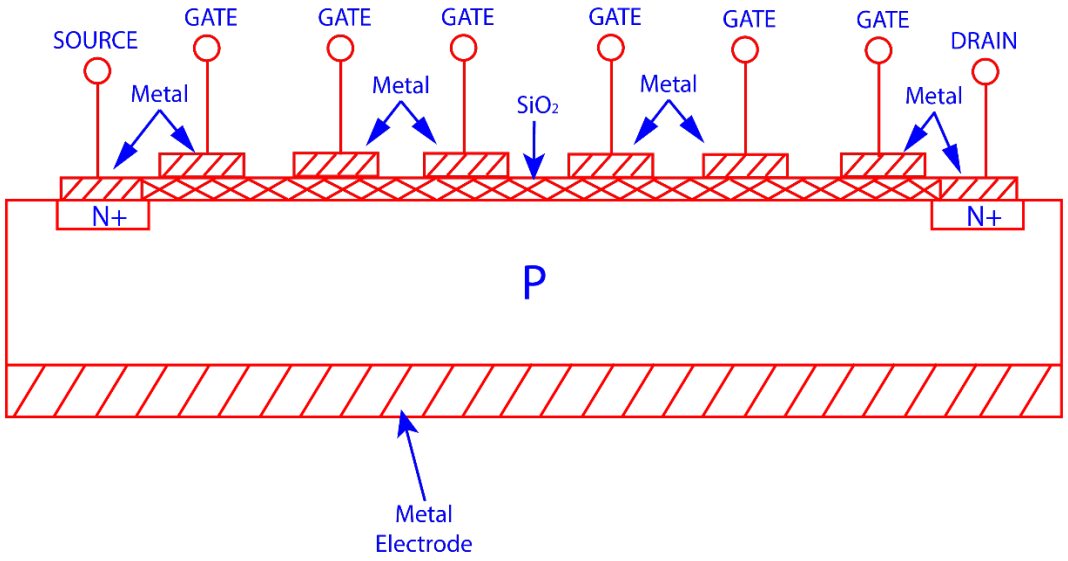


Figure 4. A simplified schematic of a "Grayzel MOSFET"

Figure 5 shows a "Grayzel MOSFET" with a drain voltage of five volts, biased such that each C-MOS capacitor has five volts across it. The bias network consists of a ten-volt DC voltage source and six resistors which can be etched onto the chip. The CCD has a structure similar to a MOSFET with a segmented gate and thus the fabrication of the "Grayzel MOSFET" is within the state of the art.

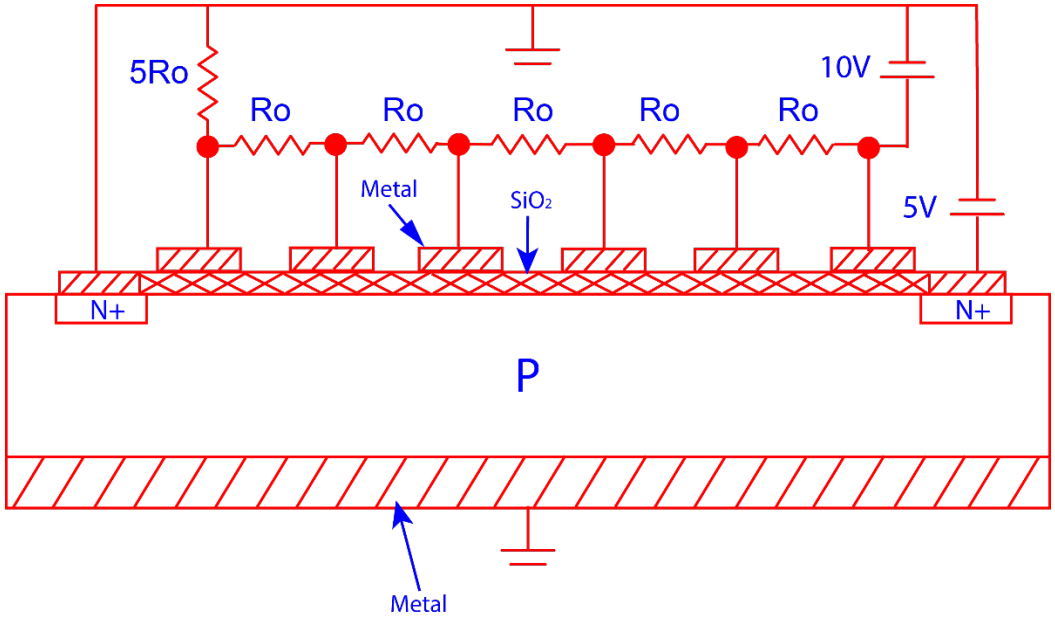


Figure 5. The "Grayzel MOSFET" with a biasing network

3: Analysis – Special case

We will consider the special case where the odd harmonics are short- circuited and the even harmonics are open-circuited and where for half of the cycle the "Grayzel FET" is cutoff and for the other half of the cycle the depletion region in the channel is of minimal width. The conductance is thus a square wave varying between 0 and G0, where G0 is the conductance when the depletion region in the channel is of minimal width. Let $\theta=2\pi ft=\omega t$, where f is the fundamental frequency of the square wave. The Fourier series of the square wave is given by:

$$G(t) = .5G0 + g(t) \quad (1a)$$

where,

$$g(t) = (2G0/\pi)(\cos\theta - \cos(3\theta)/3 + \cos(5\theta)/5 - \cos(7\theta)/7 + \ldots$$

$$= (2G0/\pi)\sum_{k=1}^{\infty}(-1)^{k-1} \cos((2k-1)\theta)/ (2k-1) \quad (1b)$$

The FET is terminated in an admittance $Y(\omega)$ which at the fundamental frequency has a value G_L. The value of $Y(\omega)$ is zero at the even harmonics of the fundamental frequency and infinite at the odd harmonics. The drain voltage therefore has only even harmonics and the drain current odd harmonics.

It is shown in [2] that the output power at the fundamental frequency P1 is given by:

$$P1 = .5(GL)(V_1)^2 = (2(V0)^2(GL)/\pi^2)/(X+(2/\pi)^2)^2 \quad (2)$$

And the efficiency EFF given by:

$$EFF=P1/P0 = (2/\pi)^2/(X+(2/\pi)^2) \quad (3)$$

Figure 6 shows a plot of the efficiency as a function of X as given by (3).

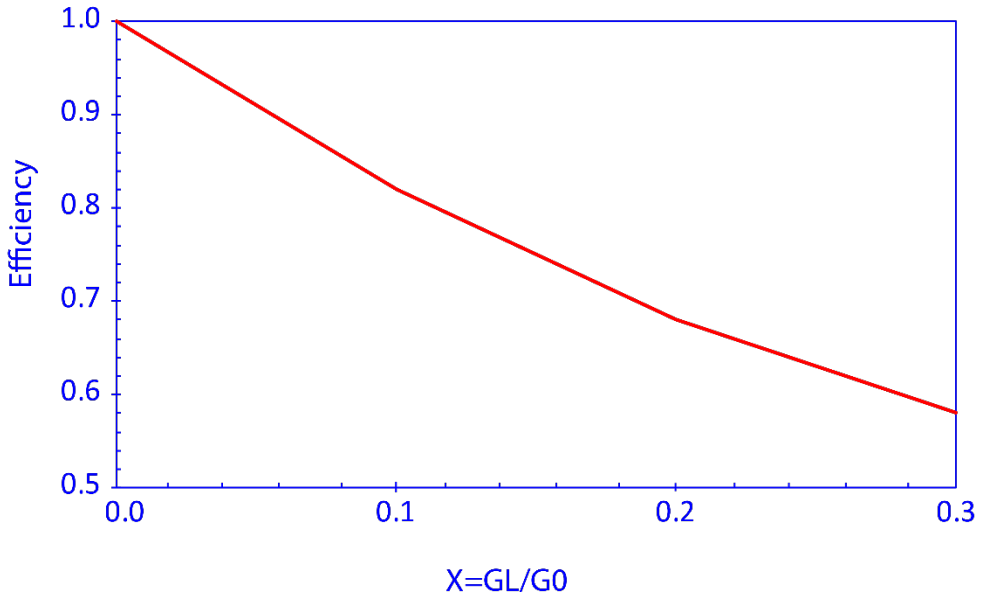


Figure 6. Efficiency as a function of X

This special case where the amplifier is terminated in an open circuit for the even harmonics and a short circuit for the odd harmonics gives good results however, it is not necessarily the optimum termination. An analysis similar to the one performed above, for the special case where the amplifier is terminated in an open circuit for the odd harmonics and a short circuit for the even harmonics gave a poorer result. An optimization needs to be done to determine the optimum termination.

4: Conclusion:

An FET will have greater efficiency and output power if pinchoff is avoided and the depletion region is made uniform along the channel. Biasing networks have been presented for achieving this condition for an FET whose gate is segmented. The efficiency and output power have been presented for the case where the odd harmonics are short circuited and the even harmonics are open circuited and where for half of the cycle the "Grayzel FET" is cutoff and for the other half of the cycle the depletion region in the channel is of minimal width**.**

5: Acknowledgement

The author wants to acknowledge the support given to my research by Dr. Ashok Gorwara CEO and the support given to me by the staff of Planar Monolithics Industries, Inc.

6: References

[1] R. F. Pierret, *Field Effect Devices. Modular Series on Solid State Devices* : Addison-Wesley Publishing Company, 1983, pp .5-15.

[2] A. I. Grayzel, "Analyze RF JFETS for Large-Signal Behavior," Microwave & rf February 2017, pp 50-55. (Available at: pmi-rf.com/tech-papers.htm)