

# **A Non-Linear Analysis of the Saturated JFET and MOSFET**

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Abstract -- The maximum power and the maximum efficiency at the maximum power have been derived for the JFET and MOSFET using the non-linear equations that describe the physics of the device. The effect of saturation and the limits of the JFET due to saturation are presented and a new JFET and MOSFET is proposed which can be biased such that it does not saturate. Analysis of this new JFET is presented and its performance compared to that of the standard JFET.

## **1. Introduction.**

RF power amplifiers are commonly analyzed by considering their output circuits without regards to the physics of the field effect transistor (FET) or the bipolar junction transistor (BJT) that is utilized. As a result, waveforms have been derived, which cannot be realized by an FET or BJT. Inspection of the transistor curves of the FET or BJT indicate that when the drain or collector voltage is zero the drain or collector current is zero since the curves all start at the origin. The class-F waveforms shown in Fig.1 and the Class-E waveforms shown in Fig. 2 have current flowing for half of the cycle while the voltage is zero and thus cannot be realized by an FET or a BJT.

In a 1967 paper Snyder [1] claimed that the Class-F waveforms shown in Fig. 1 could be realized using a Bipolar Junction Transistor (BJT). He reasoned that by applying a sinusoidal voltage between the emitter and the base the transistor would be cutoff for half the cycle and assuming that the collector current is equal to the emitter current the collector current would be that shown in Fig. 1. Further, if the load impedance short circuited all of the even harmonics and presented an open circuit to all of the odd harmonics the collector voltage would be that shown in Fig. 1 and the efficiency would be 100%. This reasoning however is not correct since the base-collector diode of a BJT must be back-biased; collector current does not flow when the collector voltage is zero. The collector current cannot drive the collector voltage to zero as the transistor will saturate and the  $\beta$  of the transistor will decrease from approximately .99 to a much smaller value. Thus the Class-F waveforms shown in Fig.1 cannot be realized by a BJT.

Sokal [2] proposed the Class-E power amplifier where the BJT operates as an on/off switch. The amplifier is analyzed with a switch that is either on; with zero voltage across it, or off; with zero current through it. This does not properly represent a BJT in the switching mode since when the BJT is switched on the collector voltage is not zero. Thus the current and voltage waveforms for Class-E shown in Fig. 2 [3], [4], [5] are not realizable with a BJT.

The waveforms shown in Fig. 1 and Fig. 2 cannot be realized by an FET as claimed by Raab [6], [7]. The current density in the channel of an FET is given by:

$$j =qnE \tag{1}$$

where  $j$  is the current density,  $q$  is the electronic charge and  $E$  is the Electric field. When the drain voltage is zero the electric field in the channel is zero and hence the current density is zero everywhere in the channel. Thus the drain current is zero when the drain voltage is zero as should be evident from the transistor curves for the FET which all start at the origin.

Cripps [8] analyzes FET amplifiers making the assumption that “This is an ideal strongly nonlinear trans conductive device, represented here as a voltage controlled current source with zero output conductance and zero turn-on (or knee) voltage.” The assumption of zero turn-on voltage means that drain current can flow when the drain voltage is zero. The waveforms presented under this assumption, for Class A [9], Class-B [10], Class-AB [11], Class-F [12], Class-D [13], Class-E [14] all have maximum drain current flowing when the drain voltage is zero and hence cannot be realized by an FET. It should be emphasized that waveforms which have current flowing when the voltage is zero cannot be realized by a BJT or FET.

The belief that an efficiency of 100% can be realized, by properly terminating an FET, disincenitized researchers from further analysis of the FET. Effort was therefore concentrated on synthesizing the terminating impedance [3], [4], [15], [16] [17], [18], [19],[20] and [21]. Raab claimed [22], [23] that by terminating all of the odd harmonics in open circuits and all of the even harmonics 100% efficiency is realized. He then analyzes the effect of terminating a limited number of harmonics [24]. Countless numbers of articles describe amplifiers which are claimed to be or class-F amplifiers [25], [26]. [27], [28]. These amplifiers were terminated in an impedance which, + open-circuits odd harmonics and short circuits even harmonics. This termination appears to enhance the efficiency of the amplifier but cannot produce the class-F waveforms. Countless numbers of articles also describe amplifiers which are claimed to be class-E amplifiers [3], [29], [30], [31], [32], [33]. While the Class-E termination has given good efficiency, it cannot produce the class-E waveforms.

In this paper the n-type JFET and the MOSFET amplifier are analyzed utilizing the non-linear equations that describe the physics of these devices, for the case where the FET is in saturation for the entire cycle. This case is easily analyzed since in saturation the drain current is only a function of the gate voltage and not a function of the drain voltage [24]. Thus for a given input excitation the drain current can be calculated as a function of time and the Fourier component at the fundamental frequency  $I_1$  can be calculated. The output power can then be calculates as  $I_1^2 R_L/2$  where  $R_L$  is the load resistance. To achieve maximum output power and efficiency  $R_L$  should be as large as possible without breaking down the FET. For a given value of  $R_L$  the maximum power will be achieved when the FET is saturated over the entire cycle, since if for part of the cycle the FET is not in saturation the drain current will be less than the saturation current for that part of the cycle and  $I_1$  will thus be reduced. The maximum power

and the maximum efficiency at the maximum power are derived for the n-type JFET and the MOSFET for three cases: the gate voltage is a sinusoid, a half sinusoid and a square wave. The maximum power and efficiency are compared for the three excitations. The effect of saturation and the limits of the FET due to saturation are presented and a new FET is proposed which can be biased such that it does not saturate. Analysis of this new FET is presented and its performance compared to that of the standard FET.

## 2. The JFET: Sinusoidal Input Voltage Excitation

The first case considered is the sinusoidal case where  $V_g$  is given by Eq. 2.

$$V_g = (V_p/2)[1 - K\cos(\omega t)] \quad (2)$$

When  $K$  equals unity the gate voltage has a maximum value of zero and minimum value of  $V_p$  ( $V_p < 0$ , for an n-type JFET). When the drain voltage of a JFET is greater than or equal to the saturated drain voltage  $V_{dsat}$ , where  $V_{dsat} = V_g - V_p$  [34] is the voltage at which pinchoff first occurs, the drain current is given by Eq. 3 [34]:

$$I_{ds} = G_0 (V_g - V_p - (2/3)(V_{bi} - V_p)\{1 - [(V_{bi} - V_g)/(V_{bi} - V_p)]^{3/2}\}) \quad (3)$$

where  $G_0$  is the conductance of the JFET's channel when there is no depletion layer,  $V_g$  is the gate voltage,  $V_p$  is the pinchoff voltage and  $V_{bi}$  is the "built-in" p-n junction potential.

As can be seen from Eq. 3, in saturation, the drain current,  $I_{ds}$ , is solely a function of the gate voltage and is not a function of the load. The drain current given by Eq. 2 can be approximated by Eq. 4 [34]:

$$I_{ds} = I_{dss}(1 - V_g/V_p)^2 \quad (4)$$

where,  $I_{dss}$  is the maximum saturated drain current which is given by Eq. 3 with  $V_g$  set equal to zero when the gate voltage is given by eq. 2 with  $K$  equal to 1. Substituting Eq. 2 into Eq. 4 yields Eq. 5:

$$\begin{aligned} I_{ds} &= I_{dss}[I_0 + I_1\cos(\omega t) + I_2\cos(2\omega t)] \\ &= I_{dss}[(2+K^2)/8 + (K/2)\cos(\omega t) + (K^2/8)\cos(2\omega t)] \end{aligned} \quad (5)$$

When  $K$  is equal to unity, Eq. 5 yields a DC current  $I_0$ , equal to  $(3/8)I_{dss}$  and a current at the fundamental frequency equal to  $I_{dss}/2$ . The DC power is then given by Eq. 6:

$$P_0 = I_0 I_{dss} V_0 = (3/8)I_{dss} V_0 \quad (6)$$

where  $V_0$  is the DC bias voltage. The output power at the fundamental frequency  $P_1$ , is given by Eq. 7:

$$P_1 = (I_{dss} I_1)^2 R_L / 2 \quad (7)$$

where  $R_L$ , is the load resistance. In saturation  $I_{ds}$  is only a function of the gate voltage  $V_g$  and thus it is not a function of the load impedance. The drain voltage is equal to the product of the drain current and the load impedance but has no effect on the drain current when the JFET is in saturation. If the load impedance presents a short-circuit at all of

the harmonics, only voltage at the fundamental frequency will appear across the load resistor. The output voltage is then  $[.5(I_{dss})R_L]K\cos(\omega t)$  when the gate voltage is equal to  $(V_p/2)[1 - K\cos(\omega t)]$  and thus, the amplifier is linear.

If  $V_g$  has a maximum value of zero and the harmonics are short circuited to ground, then for a given value of  $V_0$  the constraint that the JFET is in saturation over the entire cycle requires that the amplitude of the fundamental frequency can be no greater than  $V_0 - |V_p|$ . The minimum value of the drain voltage is then equal to  $|V_p|$  and the maximum value is equal to  $2V_0 - |V_p|$ . For the sinusoidal case with  $K$  equal to 1, the drain current flowing through the load resistor has a value  $I_1 I_{dss}$  and the load resistance  $R_L$  is then given by Eq. 8:

$$R_L = (V_0 - |V_p|) / (I_1 I_{dss}) \quad (8)$$

Solving Eq. 8 for  $V_0$  yields Eq.9

$$V_0 = (I_1 I_{dss}) R_L + |V_p| \quad (9)$$

Substituting Eq. 8 into Eq. 7 yields the output power at fundamental  $P_1$ , given by Eq. 10:

$$P_1 = (I_1 I_{dss})^2 R_L / 2 = (I_1 / 2) (I_{dss}) (V_0 - |V_p|) \quad (10)$$

The output power is given by Eq. 10 where,  $I_1 / 2 = .25$ . Eq. 6 and Eq. 10 yield the efficiency given by Eq. 11:

$$\text{Eff} = P_1 / P_0 = \text{EFF0} (V_0 - |V_p|) / V_0 = (I_1 / 2 I_0) (V_0 - |V_p|) / V_0 \quad (11)$$

EFF0 defined by Eq. 11, equals  $I_1 / 2 I_0$ , which is equal to  $2/3$ .

For a given value of  $R_L$  increasing  $V_0$  does not increase the output power since the drain current is saturated. It will however increase the D.C. power and hence reduce the efficiency. Decreasing  $V_0$  on the other hand will decrease the output power since for part of the cycle the drain current will be less than the saturation current and  $I_1$  will therefore decrease. For a given value of  $R_L$ , Eqs. 9, 10 and 11 give the maximum power and the efficiency at the maximum power. The power and efficiency will be increased by increasing  $R_L$  and therefore the largest value of  $R_L$  that does not cause breakdown should be used. The p-n junction is back biased by a voltage of  $V_d - V_g$  where  $V_d$  is the drain voltage.  $V_d - V_g$  must therefore, be less than the breakdown voltage  $V_B$ . It can be seen from Eq. 4 that the maximum value of  $I_{ds}$  occurs when  $V_g$  equals zero. Since the drain voltage is equal to  $I_{ds} R_L$ , it has its maximum when  $V_g$  is equal to zero. Therefore, the maximum value of the drain voltage which is equal to  $2V_0 - |V_p|$  must be less than  $V_B$  and the inequality Eq. 12 must be satisfied.

$$V_0 < (V_B + |V_p|) / 2 \quad (12)$$

Substituting Eq.12 into Eq. 8 yields the inequality Eq. 13:

$$R_L < (V_B - |V_p|) / (2 I_1 I_{dss}) \quad (13)$$

and substituting Eq. 13 into Eq. 10, yields the inequality Eq. 14:

$$P_1 < (I_{dss})(I_1)(V_B - |V_p|) / 4 = P_{vb} (I_{dss})(V_B - |V_p|) \quad (14)$$

where  $P_{vb} = I_1 / 4 = .125$  for the sinusoidal case. Substituting Eq. 12 into Eq. 11, yields by Eq. 15:

$$\text{Eff} = P_1 / P_0 < \text{EFVb}(V_B - |V_p|) / (V_B + |V_p|) \quad (15)$$

where,  $\text{EFVb} = \text{EFF0} = I_1 / 2I_0 = 2/3$  for the sinusoidal case.

Given  $V_B$ ,  $V_p$  and  $I_{dss}$  Eq. 12 gives the value of  $V_0$  and Eq. 13 gives the value of  $R_L$  that yields maximum power with the maximum efficiency. The value of the maximum output power and the value of the efficiency at the maximum power are given by Eq. 14 and Eq. 15.

### 3. COMPUTER ANALYSIS

To test the accuracy of the approximation for  $I_{ds}$  given by Eq. 4, a simple program was written where the following instructions were performed.

- 1- Read from an input file,  $G_0$ ,  $V_p$  and  $V_{bi}$ .
- 2- Define 1,440 points by incrementing theta from 0 to 360 degrees in increments of 360/1440 degrees.
- 3- At each of these points calculate  $V_g$  given by Eq. 2 with  $K$  set equal to unity and using these values of  $V_g$ , calculate  $I_{ds}$  at these 1440 points using Eq. 3.
- 4- Calculate  $I_{dss}$  using Eq. 3 with  $V_g$  set equal to zero.
- 5- Calculate  $I_{ds}/I_{dss}$  at these 1440 points and plot  $I_{ds}/I_{dss}$ .
- 6- Calculate the Fourier Coefficients  $I_0$  and  $I_1$ , using Simpsons rule.
- 7- Calculate  $\text{EFF0} = I_1/2I_0$ .

The results are shown for six cases in Table 1. The approximate value of  $\text{EFF0}$  calculated using Eq. 11 is within 0.5% of the value calculated using Eq. 4. Figure 3 shows the plots of  $I_{ds}/I_{dss}$  as a function of THETA for all six cases. They are so close to one another that they appear as a thickened curve.  $I_{ds}/I_{dss}$  calculated using Eq. 4 and Eq. 2 is also plotted in Figure 3.

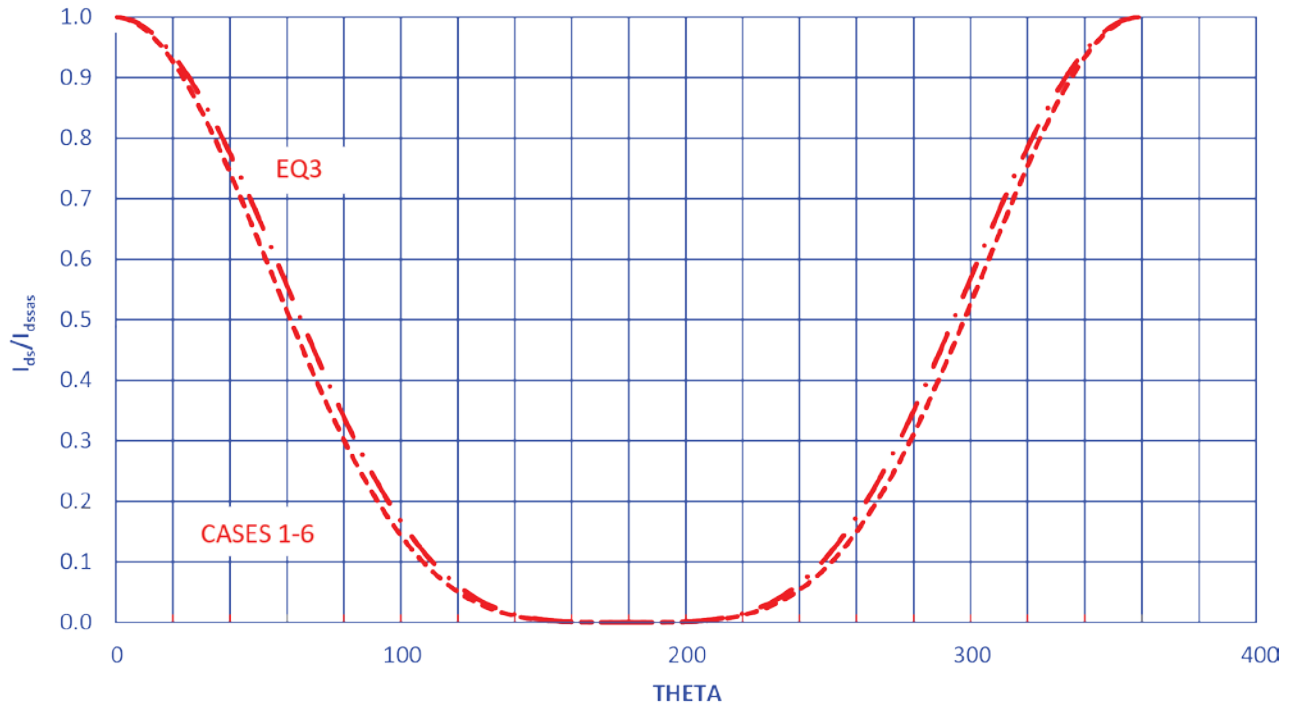


Figure 3.  $I_{ds}/I_{dss}$  as a function of  $\theta$  computed using Eq. 3 and six cases analyzed by computer program.

Case	$G_0$	$V_p$	$V_{bi}$	$I_0$	$I_1$	EFF0	$I_2$
1	0.0072	-2.908	0.859	0.3616	0.4920	0.6695	0.1373
2	0.0086	-3.656	0.864	0.3604	0.4912	0.6694	0.1383
3	0.0101	-4.405	0.868	0.3594	0.4904	0.6693	0.1391
4	0.0115	-5.155	0.871	0.3586	0.4898	0.6691	0.1397
5	0.0288	-6.656	0.877	0.3573	0.4889	0.6689	0.1407
6	0.0576	-29.219	0.913	0.3521	0.4845	0.6668	0.1441

Table 1.

#### 4. The Half Sinusoidal Input Voltage Excitation

The second case to be considered is the half sinusoidal case. For half of the cycle  $V_g/V_p$  is a sinusoid and for the other half of the cycle  $V_g$  is equal to  $V_p$ .  $V_g/V_p$  is given by Eq. 16.

$$V_g/V_p = 1 - \cos(\omega t) \quad -90^\circ < \omega t < 90^\circ$$

$$V_g/V_p = 1 \quad \text{otherwise} \quad (16)$$

Substituting  $V_g/V_p$  into Eq. 4 yields:

$$I_{ds}/I_{dss} = (\cos(\omega t))^2 \quad -90^\circ < \omega t < 90^\circ$$

$$I_{ds} / I_{dss} = 0 \quad \text{otherwise} \quad (17)$$

$V_g / V_p$  was chosen such that  $I_{ds} / I_{dss}$  has its a maximum at  $\omega t = 0$  and can be represented by the product of  $\text{Cos}^2(\omega t)$  and a square wave of unit magnitude centered on  $\omega t = 0$ . Using the Fourier expansion of the square wave and the trigonometric identity for  $\text{Cos}^2(\omega t)$ ,  $I_{ds} / I_{dss}$  can be written as:

$$I_{ds} / I_{dss} = .5(1 + \text{Cos}(2\omega t))(.5 + (2/\pi)(\text{Cos}(\omega t) - \text{Cos}(3\omega t)/3 + \text{Cos}(5\omega t)/5...)) \quad (18)$$

Multiplying the two factors and using the trigonometric identity for the product of two cosines yields Eq. 19.

$$I_{ds} / I_{dss} = .25 + (4/3\pi)\text{Cos}(\omega t) + (.25) \text{Cos}(2\omega t) + (4/15\pi)\text{Cos}(3\omega t) + \quad (19)$$

It can be seen from Eq. 19 that  $I_1$  is equal to  $4/3\pi$  and  $I_0$  is equal to  $.25$ . The DC power is given by Eq. 20;

$$P_0 = I_0 I_{dss} V_0 = I_{dss} V_0 / 4 \quad (20)$$

As discussed above the load impedance should present a short-circuit at all of the harmonic frequencies and the constraint that the JFET is in saturation over the entire cycle requires that the amplitude of the fundamental frequency can be no greater than  $V_0 - |V_p|$ . The minimum value of the drain voltage is then equal to  $|V_p|$  and the maximum value is  $2V_0 - |V_p|$ . The drain current flowing through the load resistor is then sinusoidal and has a value equal to  $(4/3\pi)I_{dss}$  at the fundamental frequency. The load resistance  $R_L$  is given by Eq. 8 and  $V_0$  by Eq. 9. Substituting the value of  $I_1$  into Eq. 10, yields Eq. 21.

$$P_1 = I_{dss} (4/3\pi) (V_0 - |V_p|) / 2 = I_{dss} (.211) (V_0 - |V_p|) \quad (21)$$

With  $I_1 = 4/3\pi$  and  $I_0 = .25$  the efficiency; equal to  $P_1/P_0$  is given by Eq. 22.

$$\text{Eff} = \text{EFF}_0 (V_0 - |V_p|) / V_0 = (.844) (V_0 - |V_p|) / V_0 \quad (22)$$

Eqs. 21 and 22 shows that the half sine wave input excitation will give greater efficiency than the sine wave excitation but less output power.

Inspection of Eq. 16 shows that at the maximum drain voltage the value of  $V_g$  is zero and hence to avoid breakdown Eq. 12 and Eq. 13 must be satisfied. Given  $V_B$ ,  $V_p$  and  $I_{dss}$  Eq. 12 gives the value of  $V_0$  and Eq. 13 gives the value  $R_L$  that yields the maximum power with the maximum efficiency. The value of the maximum output power and the value of the efficiency at the maximum point are given by Eq. 14 and Eq. 15 where for the half sinusoidal case,  $P_{vb} = 1/3\pi = .106$  and  $\text{EFVb} = .844$ .

## 5. Square Wave Input Voltage Excitation

The third case to be considered is the square wave where for half of the cycle  $V_g/V_p$  is equal to unity and for the other half of the cycle  $V_g$  is equal to  $V_p$ .  $V_g/V_p$  is given by Eq. 23:

$$\begin{aligned} V_g/V_p &= 0 & -90^\circ < \omega t < 90^\circ \\ V_g/V_p &= 1 & \text{otherwise} \end{aligned} \quad (23)$$

Substituting  $V_g/V_p$  into Eq.4 yields:

$$\begin{aligned} I_{ds}/I_{dss} &= 1 & -90^\circ < \omega t < 90^\circ \\ I_{ds}/I_{dss} &= 0 & \text{otherwise} \end{aligned} \quad (24)$$

$V_g/V_p$  was chosen such that  $I_{ds}/I_{dss}$  is a square wave centered at  $\omega t$  equal to zero, whose Fourier series is given by Eq. 25.

$$I_{ds}/I_{dss} = (.5 + (2/\pi)\text{Cos}(\omega t) - (2/3\pi)\text{Cos}(3\omega t) + (2/5\pi)\text{Cos}(5\omega t)) \dots\dots\dots (25)$$

It can be seen from Eq. 25 that  $I_1$  is equal to  $2/\pi$  and  $I_0$  is equal to .5.

As discussed above the load impedance should present a short-circuit at all of the harmonic frequencies and the constraint that the JFET is in saturation over the entire cycle requires that the amplitude of the fundamental frequency can be no greater than  $V_0 - |V_p|$ . The minimum value of the drain voltage is then equal to  $|V_p|$  and the maximum value is  $2V_0 - |V_p|$ . The drain current flowing through the load resistor is then sinusoidal and has a value equal to  $(2/\pi)I_{dss}$ . The load resistance  $R_L$  is given by Eq. 8 and  $V_0$  by Eq. 9. Substituting the value of  $I_1$  into Eq. 10, yields Eq. 26.

$$P_1 = I_{dss} (2/\pi) (V_0 - |V_p|)/2 = I_{dss} (.317) (V_0 - |V_p|) \quad (26)$$

Since  $P_0 = I_0 I_{dss} V_0$  The efficiency equal to  $P_1/P_0$  is given by Eq. 27.

$$\text{Eff} = \text{EFF0}(V_0 - |V_p|)/V_0 = (.634)(V_0 - |V_p|)/V_0 \quad (27)$$

Inspection of Eq. 23 and Eq. 24 shows that at the maximum drain voltage the value of  $V_g$  is zero and hence to avoid breakdown Eq. 12 and Eq. 13 must be satisfied. Given  $V_B$ ,  $V_p$  and  $I_{dss}$  Eq. 12 gives the value of  $V_0$  and Eq. 13 gives the value  $R_L$  that yields the maximum power with the maximum efficiency.

The value of the maximum output power and the value of the efficiency at the maximum power are given by Eq. 14 and Eq. 15 where for the square wave case,  $P_{vb} = 1/2\pi = .159$  and  $\text{EFVb} = .634$ .

Comparison of the values of  $\text{EFF0}$  and  $P_{vb}$  for the sine wave and half sine wave and square wave cases show that the square wave input excitation gives the greatest output power while the half sine wave input excitation gives the greatest efficiency.



## 6. Analysis of the Results

To understand the results let us examine the behavior of the JFET in saturation. When the drain voltage of a JFET is exactly equal to the saturated drain voltage,  $V_{dsat}$ , the conditions are those of Figure 4(a) where pinchoff occurs exactly at the drain of the transistor [35]. If the drain voltage is increased by  $\Delta V$ , the point at which pinchoff occurs moves towards the source a distance of  $\Delta L$ , as shown in Figure 4(b). Over the length  $\Delta L$ , the channel is completely depleted; only minority carriers remain and the resistance is quite large. Voltage  $\Delta V$  is dropped across this depleted region and due to the high resistivity in the depleted region,  $\Delta L$  is very small. For  $\Delta L \ll L$ , which represents the usual case, the depletion from source to pinchoff point will be essentially identical in shape and the channel will have essentially the same resistance from the source to the point where pinchoff now occurs. The drain current, which is equal to  $V_{dsat}$  divided by this resistance, hardly changes. This explains why the value of the drain current is nearly constant for drain voltages greater than  $V_{dsat}$ . Since voltage  $\Delta V(t)$  is dropped across the depleted region  $\Delta L$ , it does not contribute to the output power and simply degrades the efficiency. It is therefore clear that, for high efficiency, the depletion region must be minimized and pinch-off avoided. Ideally, for converting DC power to RF power, the channel should have no depletion at all for one-half the cycle and should be completely cut-off for the other one-half cycle. With the optimum load, this should yield the maximum DC-to-RF efficiency. To accomplish this, a new (patent pending) JFET is proposed, which will be referred to as the ‘‘Grayzel JFET.’’

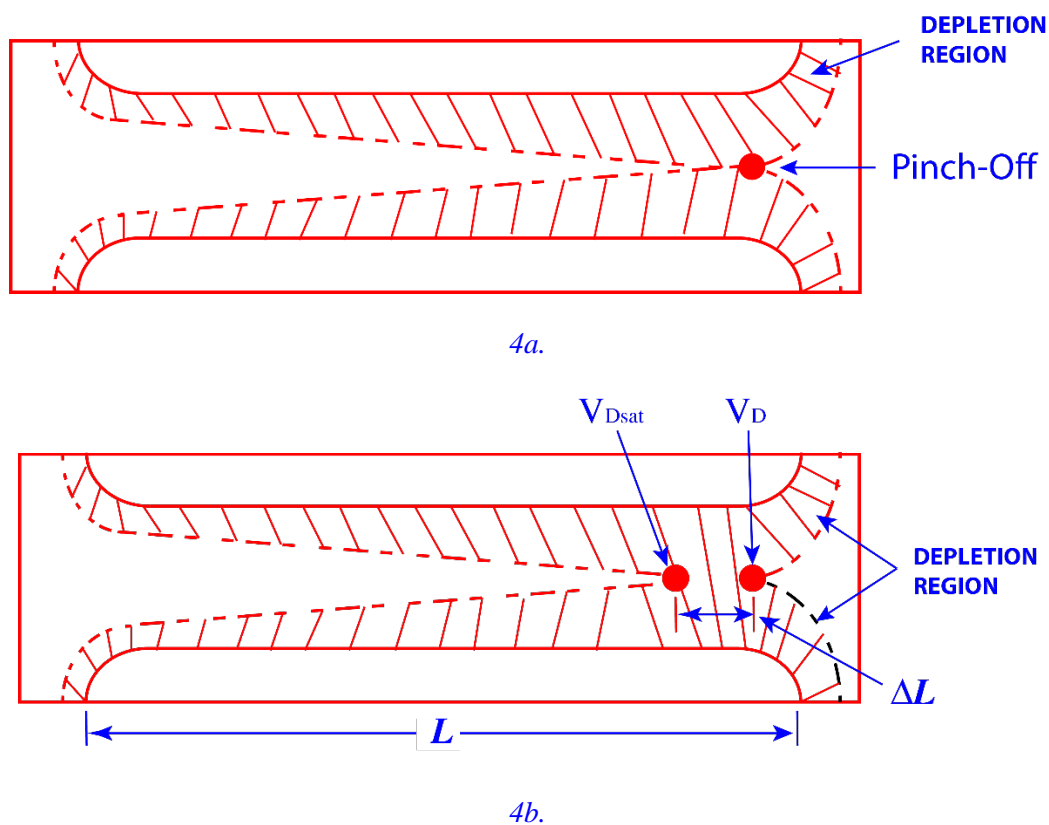


Figure 4. The diagrams show the channel of a JFET under different conditions: (a) when the drain voltage equals the pinchoff voltage and (b) when the drain voltage exceeds the pinchoff voltage.

## 7. The “Grayzel JFET”

Figure 5 shows a simplified schematic of a JFET with a drain voltage of 7 V dc. Along the channel, the potential has values of 0, 1, 2, 3, 4, 5, 6, and 7 V. The junction is progressively back-biased, causing greater depletion at the drain than at the source. Figure 6 shows a simplified schematic diagram of the “Grayzel JFET.” The p+ region is divided into N sections that are insulated from one another, forming N, p-n junctions. (In Figure 6, N is equal to 8 as an illustrative example.) Each p-n junction is biased to ground separately as shown in Figure 6; the first at  $V_0$  and the eighth at  $V_0 + 7$ . With a drain voltage of 7 V, all of the p-n junctions will have the same DC voltage  $V_0$  across their junctions and hence, to a good approximation the width of the depletion region at each of the p-n junctions will be the same.

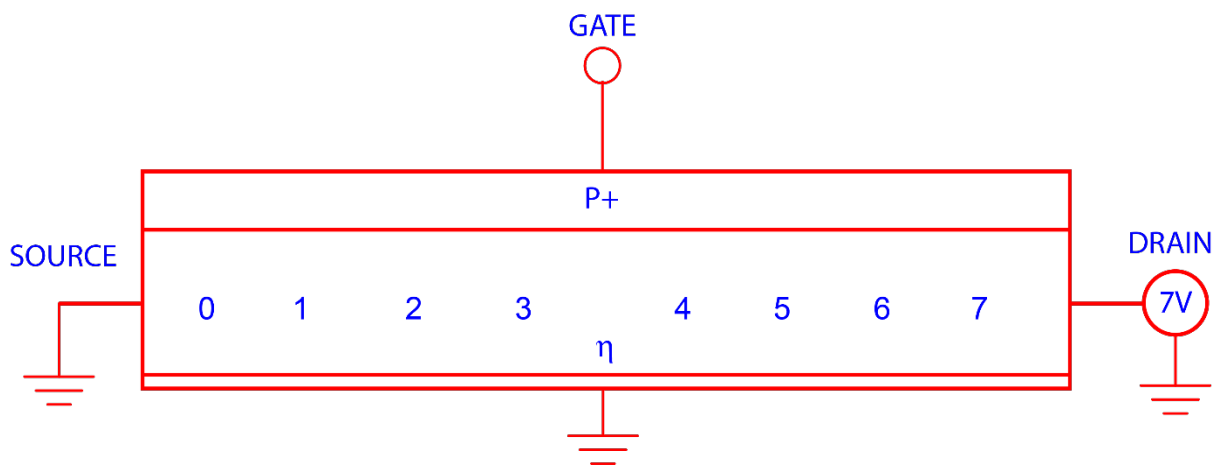


Figure 5. Voltage Drop Down the Channel of a JFET for a Drain Voltage of 7 Volts.

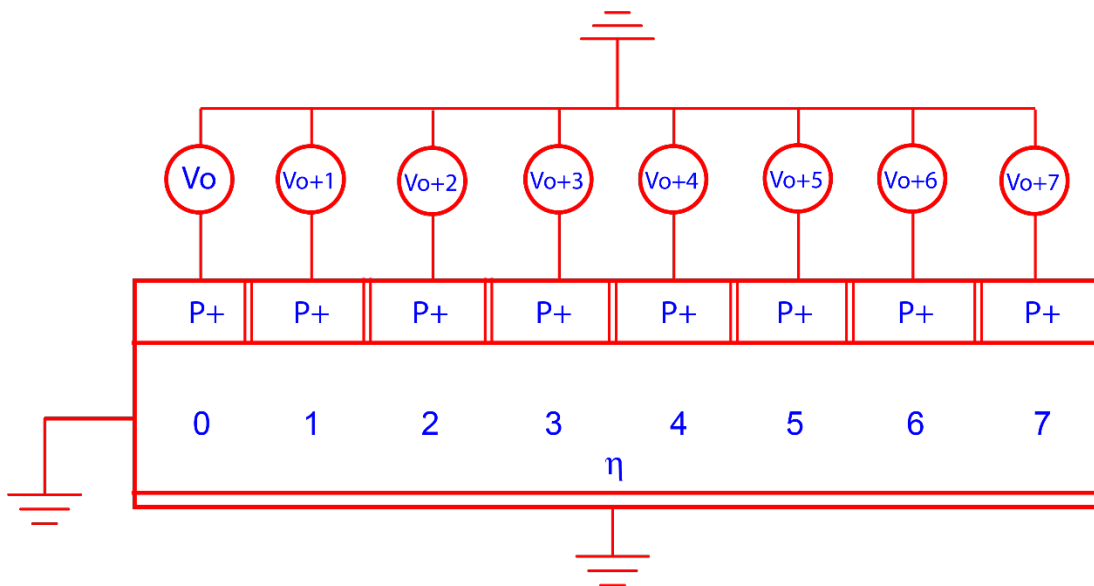


Figure 6. A “Grayzel JFET” where the p-n junctions are individually biased such that each p-n junction is reverse biased at voltage  $V_0$ .

Let us consider as an example a Grayzel JFET where all of the p-n junctions are completely depleted when back-biased with a voltage of -4 V dc. When the gate voltage is equal to -4 V dc, the drain current is approximately zero. A square wave varying from -2 to +2 V is applied to each of the p-n junctions through an eight-way, in-phase power divider as shown in Figure 7 and the p-n junctions are biased such that each p-n junction is back biased by a voltage of -2 V dc when the drain voltage is equal to 7 V dc. The channel will be approximately without depletion for one-half of the cycle and cutoff for the other one-half of the cycle. For very large N, the conductance of the channel approaches an ideal square wave varying between 0 and  $G_0$ , where  $G_0$  is the value of the conductance of the channel when the gate voltage is equal to zero. Biasing the gate such that the channel is cutoff for half the cycle and without a depletion layer for half the cycle should provide the highest efficiency. Dividing the gate into multiple sections is applicable to all types of FETs. Figure 8 shows an example of the (patent pending) “Grayzel MOSFET” with the gate divided into N sections, with  $N = 6$ .

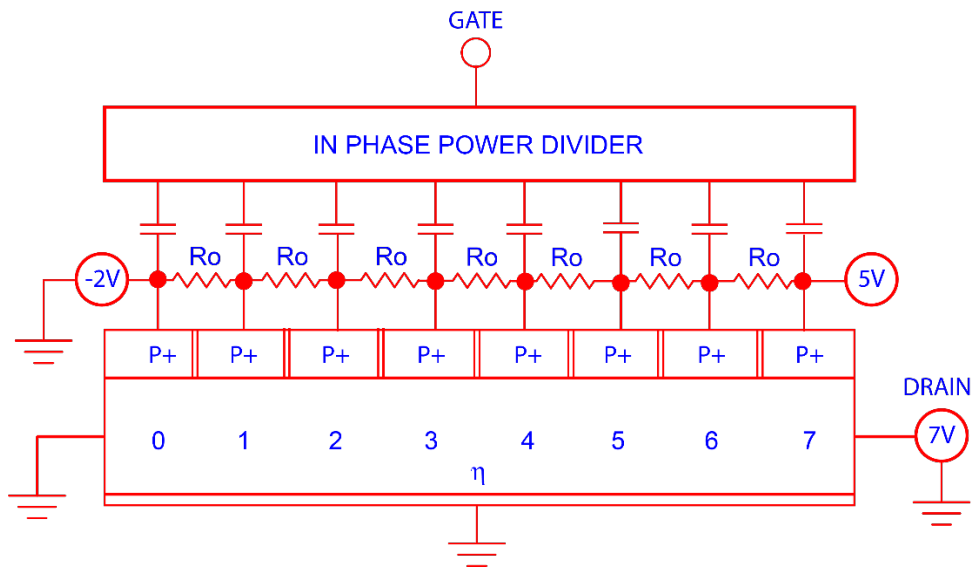


Figure 7. A simplified schematic of a “Grayzel JFET” where each p-n junction is biased at -2 Vdc

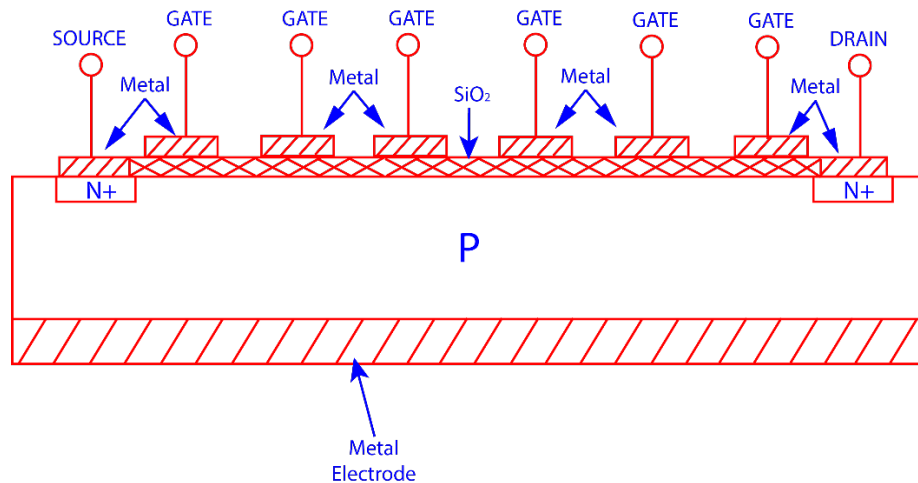


Figure 8. A simplified schematic of a “Grayzel MOSFET”

Terminating the “Grayzel JFET” in a load impedance that short-circuits the odd-order harmonics and open-circuits the even-order harmonics gives good results when the gates are biased as described above so that the conductance is a square wave varying between 0 and  $G_0$ . The performance under these conditions is analyzed in the Appendix.

## 8. Numerical Example

Let us consider an n-channel JFET where  $V_p = -6.66$  volts,  $V_{bi} = .877$  volts,  $I_{dss} = .0528$  amps and  $V_b = 30$  volts. Solving Eq. 3 with these values and  $V_g = 0$  yields  $G_0 = .0288$ . Using Eqs. 12, 13, 14, and 15 the load resistance, output power and efficiency are computed at the breakdown voltage for the three cases; case1; sinewave, case 2; half sine wave and case 3; square wave. The results are given in Table 2.

CASE	$P_1$ mw	EFF%	$R_L$ ohms
1	308	42.5	884
2	261	53.7	1041
3	392	40.4	694

Table 2.

Let us compare this with the “Grayzel JFET” with  $G_0$  equal to .0288,  $V_p$  equal to -6.66 volts, a breakdown voltage of 30 volts and the even harmonics open circuited and the odd harmonics short circuited. It was shown in the Appendix that the efficiency is given by Eq. A18 as:

$$\text{Eff} = .405/(X + .405) \quad (28)$$

where

$$X = G_L/G_0 = 1/(R_L G_0) \quad (29)$$

and the output power is given by Eq. A17 as:

$$P_1 = .5G_L[(2/\pi)V_0/(X + (2/\pi)^2)]^2 \quad (30)$$

where  $V_0$  at breakdown is given by Eq. A20 (in the Appendix) and is equal to  $(V_b - |V_p|)/I_{d180}$ .  $I_{d180}$  the maximum values of the drain voltage is plotted in Fig. A5 (in the Appendix) as a function of  $X$ .

In Table 3 the values at breakdown of the output power  $P_1$  and the efficiency are shown for values of  $R_L$  equal to 100, 350, 700 and 1000 ohms.

$R_L$	$P_1$ mw	EFF
100	403	53.9
350	166	80.3
750	83.5	89.7
1000	64	92.1

Table 3.

## 9. The MOSFET; Sinusoidal Input Voltage Excitation – Square Law Theory

There are two theories for obtaining a relationship for the drain current as a function of the gate voltage, when the MOSFET is in saturation; the square law theory and the bulk theory. In the following analysis the square law theory will be used as it is simpler and gives good insight to the performance of the MOSFET.  $I_{dsat}$  is given by Eq. 31 when using the square law theory [36].

$$I_{dsat} = (Z\mu'_n C_0/2L)(V_g - V_T)^2 \quad (31)$$

Where,  $\mu'_n$  is the average mobility of the inversion layer carriers,  $C_0$  is the oxide capacitance,  $Z$  is the width of the channel and  $L$  is its length.

The first case considered is the sinusoidal case where  $V_g$  is given by Eq. 32.

$$V_g = (V_{gmax} + V_T)/2 + [(V_{gmax} - V_T)/2] \text{Cos}(\omega t) \quad (32)$$

$V_g$  has a maximum value of  $V_{gmax}$  and a minimum value of  $V_T$ . Substituting Eq. 32 into Eq. 31 yields:

$$I_{dsat} = (Z\mu'_n C_0/2L)[(V_{gmax} - V_T) (1 + \text{Cos}(\omega t)) /2]^2 \quad (33)$$

$I_{dss}$ , the maximum saturated drain current, is given by Eq. 31 with  $V_g$  set equal to  $V_{gmax}$ .

$$I_{dss} = (Z\mu'_n C_0/2L)(V_{gmax} - V_T)^2 \quad (34)$$

Dividing Eq. 33 by Eq. 34 yields Eq. 35.

$$\begin{aligned} I_{dsat}/I_{dss} &= (1 + \text{Cos}(\omega t)) /2]^2 \\ &= 3/8 + 1/2 \text{Cos}(\omega t) + 1/8 \text{Cos}(2 \omega t) \end{aligned} \quad (35)$$

Eq. 35 yields a DC current  $I_0$ , equal to  $(3/8)I_{dss}$  and a current at the fundamental frequency equal to  $I_{dss}/2$ .

The DC power is given by Eq. 36

$$P_0 = I_0 I_{dss} V_0 = (3/8)I_{dss} V_0 \quad (36)$$

where  $V_0$  is the DC bias voltage. The output power at the fundamental frequency  $P_1$ , is given by Eq. 37:

$$P_1 = (I_{dss} I_1)^2 R_L / 2 \quad (37)$$

The drain current is not a function of the load impedance when the MOSFET is in saturation and since only the fundamental frequency is desired at the output, the load impedance should present a short-circuit at all of the harmonic frequencies. Only voltage at the fundamental frequency will then appear across the load resistor and it is in phase with the drain current. Since  $V_{dsat}$  is equal to  $(V_g - V_T)$  for a MOSFET[36], for a given value of  $V_0$  the constraint that the MOSFET is in saturation over the entire cycle and the harmonics are short circuited to ground requires that the amplitude of the fundamental frequency can be no greater than  $V_0 - (V_{gmax} - V_T)$ . The minimum value of the drain voltage is then equal to  $(V_{gmax} - V_T)$  and the maximum value is equal to  $2V_0 - (V_{gmax} - V_T)$ . Since the drain current flowing through the load resistor is sinusoidal and has a value  $I_1 I_{dss}$ , the load resistance is given by Eq. 38.

$$R_L = (V_0 - (V_{gmax} - V_T)) / (I_1 I_{dss}) \quad (38)$$

Solving Eq. 38 for  $V_0$  yields Eq. 39

$$V_0 = (I_1 I_{dss}) R_L + (V_{gmax} - V_T) \quad (39)$$

Substituting Eq. 38 into Eq. 37 yields the output power at fundamental-frequency,  $P_1$ , given by Eq. 40:

$$P_1 = (I_1 I_{dss})^2 R_L / 2 = (I_1 I_{dss}) (V_0 - (V_{gmax} - V_T)) / 2 \quad (40)$$

and the output power is given by Eq. 41.

$$P_1 = .25 (I_{dss}) (V_0 - (V_{gmax} - V_T)) \quad (41)$$

The efficiency is given by Eq. 42:

$$Eff = P_1 / P_0 = EFF0 (V_0 - (V_{gmax} - V_T)) / V_0 = (I_1 / 2I_0) (V_0 - (V_{gmax} - V_T)) / V_0 \quad (42)$$

$EFF0$  equals  $I_1 / 2I_0$ , which is equal to  $2/3$  for the sinusoidal case.

For a given value of  $R_L$  increasing  $V_0$  does not increase the output power since the drain current is saturated. It will however increase the D.C. power and hence reduce the efficiency. Decreasing  $V_0$  on the other hand will decrease the output power since for part of the cycle the drain current will be less than the saturation current. For a given value of  $R_L$ , Eqs. 39, 41 and 42 give the maximum power and the efficiency at the maximum power. The power and efficiency will be increased by increasing  $R_L$ , but is limited by the breakdown voltage of the p-n junction at the drain.

## 10. The MOSFET; The Half Sinusoidal Input Voltage Excitation

The second case to be considered is the half sinusoidal case. For half of the cycle  $V_g$  is a sinusoid with a maximum value of  $V_{gmax}$  and a minimum of  $V_T$  and for the other half of the cycle  $V_g$  is equal to  $V_T$ .  $V_g$  is given by Eq. 43.

$$\begin{aligned} V_g &= V_T + (V_{gmax} - V_T)\text{Cos}(\omega t) & -90^\circ < \omega t < 90^\circ \\ V_g &= V_T & \text{otherwise} \end{aligned} \quad (43)$$

Substituting  $V_g$  into Eq.31 and dividing by Eq. 34 yields

$$\begin{aligned} I_{ds}/I_{dss} &= \text{Cos}^2(\omega t) & -90^\circ < \omega t < 90^\circ \\ I_{ds}/I_{dss} &= 0 & \text{otherwise} \end{aligned} \quad (44)$$

$I_{ds}/I_{dss}$  can be represented by the product of  $\text{Cos}^2(\omega t)$  and a square wave of unit magnitude centered at  $\omega t=0$ . Using the Fourier expansion of the square wave and the trigonometric identity for  $\text{Cos}^2(\omega t)$ ,  $I_{ds}/I_{dss}$  can be written as:

$$I_{ds}/I_{dss} = .5(1+\text{Cos}(2\omega t))(.5 + (2/\pi)(\text{Cos}(\omega t) - \text{Cos}(3\omega t)/3 + \text{Cos}(5\omega t)/5\dots)) \quad (45)$$

Multiplying the two factors and using the trigonometric identity for the product of two cosines yields Eq. 46.

$$I_{ds}/I_{dss} = .25 + (4/3\pi)\text{Cos}(\omega t) + (.25)\text{Cos}(2\omega t) + (4/15\pi)\text{Cos}(3\omega t) + \dots \quad (46)$$

It can be seen from Eq. 45 that  $I_1$  is equal to  $4/3\pi$  and  $I_0$  is equal to .25. The DC power is given by Eq. 47;

$$P_0 = I_0 V_0 = I_{dss} V_0/4 . \quad (47)$$

Since the drain current is not a function of the load impedance when the MOSFET is in saturation and only the fundamental frequency is desired at the output the load impedance should present a short-circuit at all of the harmonic frequencies. Only voltage at the fundamental frequency will then appear across the load resistor and it is in phase with the drain current. For a given value of  $V_0$  the load resistance  $R_L$  is given by Eq. 38 and  $V_0$  by Eq. 39 for the constraint that the MOSFET is in saturation over the entire cycle and the harmonics are short circuited to ground. The output power is given by Eq. 40, which for  $I_1 = 4/3\pi$  is given by Eq. 48.

$$P_1 = I_{dss} (4/3\pi) (V_0 - (V_{gmax} - V_T))/2 = I_{dss} (.212) (V_0 - (V_{gmax} - V_T)) \quad (48)$$

The efficiency equal to  $P_1/P_0$  where  $I_1 = 4/3\pi$  and  $I_0 = .25$  is given by Eq. 49.

$$\text{Eff} = \text{EFF}_0 (V_0 - (V_{gmax} - V_T))/V_0 = (.849) (V_0 - (V_{gmax} - V_T))/V_0 \quad (49)$$

Eqs. 48 and 49 show that the half sine wave input excitation will give greater efficiency than the sine wave excitation but less output power.

## 11. The MOSFET; Square Wave Input Voltage Excitation

The third case to be considered is the square wave where for half of the cycle  $V_g$  is equal to  $V_{gmax}$  and for the other half of the cycle  $V_g$  is equal to  $V_T$ .  $V_g$  is given by Eq. 50:

$$\begin{aligned} V_g &= V_{gmax} & -90^\circ < \omega t < 90^\circ \\ V_g &= V_T & \text{otherwise} \end{aligned} \tag{50}$$

Substituting  $V_g$  into Eq.31 and dividing by Eq. 34 yields

$$\begin{aligned} I_{ds}/I_{dss} &= 1 & -90^\circ < \omega t < 90^\circ \\ I_{ds}/I_{dss} &= 0 & \text{otherwise} \end{aligned} \tag{51}$$

$I_{ds}/I_{dss}$  is a square wave centered at  $\omega t$  equal to zero; whose Fourier series is given by Eq. 52.

$$I_{ds}/I_{dss} = (.5 + (2/\pi)\text{Cos}(\omega t) - (2/3\pi)\text{Cos}(3\omega t) + (2/5\pi)\text{Cos}(5\omega t) \dots\dots\dots) \tag{52}$$

It can be seen from Eq. 52 that  $I_1$  is equal to  $2/\pi$  and  $I_0$  is equal to .5.

Since the drain current is not a function of the load impedance when the MOSFET is in saturation and only the fundamental frequency is desired at the output the load impedance should present a short-circuit at all of the harmonic frequencies. Only voltage at the fundamental frequency will then appear across the load resistor and it is in phase with the drain current. For a given value of  $V_0$  the load resistance  $R_L$  is given by Eq. 38 and  $V_0$  by Eq. 39 for the constraint that the MOSFET is in saturation over the entire cycle and the harmonics are short circuited to ground. The output power is given by Eq. 40, which for  $I_1 = 4/3\pi$  is given by Eq. 53.

$$P_1 = I_{dss} (2/\pi) (V_0 - (V_{gmax} - V_T)/2) = I_{dss} (.318) (V_0 - (V_{gmax} - V_T)) \tag{53}$$

The efficiency equal to  $P_1/P_0$  is given by Eq. 54 for  $I_1 = 2/\pi$  and  $I_0 = .5$ .

$$\text{Eff} = [I_1 / (2 I_0)] [(V_0 - (V_{gmax} - V_T)/V_0)] = (.637) (V_0 - (V_{gmax} - V_T))/V_0 \tag{54}$$

Comparison of the values of EFF and  $P_1$  the sine wave, the half sine wave and square wave cases show that the square wave input excitation gives the greatest output power while the half sine wave input excitation gives the greatest efficiency.



Comparison of Eqs. 5, 18 and 25 with Eqs. 35b, 46 and 52 shows that  $I_{ds}/I_{dss}$  is the same for the JFET and the MOSFET when the square law theory is used to analyze the MOSFET.  $EFF_0$  is the same for the JFET and MOSFET for all three cases as is the output power for a given load resistance.

## 12. Conclusion

A non-linear analysis for the JFET and for the MOSFET has been presented and the maximum power and maximum efficiency at the maximum power for the JFET has been derived. The limitation of the JFET due to saturation has been explained and a new FET which does not saturate has been proposed. The performance of the new JFET and that of the present JFET is compared. The analysis presented demonstrates that the class-F waveforms are not realizable with an FET nor is any set of waveforms where drain current flows when the drain voltage is zero. It should be noted that the Class-E and the Class-F waveforms cannot be realized with a bipolar junction transistor as well, since when the collector voltage is zero, the collector current is zero.

## 13. Acknowledgements

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## APPENDIX

In this appendix the “Grayzel JFET” is analyzed for the case where the odd-order harmonics are short-circuited and the even-order harmonics are open-circuited and where for half of the cycle the “Grayzel JFET” is cutoff and for the half of the cycle centered on  $\theta = 0^\circ$  there is no depletion in the channel. The conductance  $G(t)$  is thus a square wave varying between zero and  $G_0$ , where  $G_0$  is the conductance when there is no depletion region. The conductance is given by Eq. A1:

$$G(t) = 0.5G_0 + g(t) \quad (A1)$$

where  $g(t)$  is a square wave centered on  $\theta = 0^\circ$  which varies between  $-.5G_0$  and  $.5G_0$  and is given by Eq. A2.

$$\begin{aligned} g(t) &= (2G_0/\pi)(\text{Cos}\theta - \text{Cos}(3\theta)/3 + \text{Cos}(5\theta)/5 - \text{Cos}(7\theta)/7 + \dots) \\ &= (2G_0/\pi)\sum_{k=1}^{\infty} (-1)^{k-1} \text{Cos}((2k-1)\theta) / (2k-1) \end{aligned} \quad (A2)$$

where  $\theta = 2\pi ft = \omega t$ , and  $f$  is the fundamental frequency of the square wave.

The “Grayzel JFET” is terminated in an admittance  $Y(\omega)$  which at the fundamental frequency is real and has a value  $G_L = 1/R_L$ . The value of  $Y(\omega)$  is zero at the even harmonics and infinite at the odd harmonics of the fundamental frequency. The drain voltage therefore has only even harmonics and the drain current has only odd harmonics. The drain voltage,  $V_d(t)$  will have the form of Eq. A3:

$$V_d(t) = V_0 + v(t) \quad (A3)$$

Where

$$v(t) = V_1 \text{Cos}(\theta) + \sum_{k=1}^{\infty} (V_{2k})\text{Cos}(2k\theta) \quad (A4)$$

Eq. A4 represents the voltage  $v(t)$  for the following reason. The value of the conductance of the channel is equal to  $G_0$  when  $-90^\circ < \theta < +90^\circ$  and the channel is cutoff during the remainder of the cycle. Current will therefore only flow when  $-90^\circ < \theta < +90^\circ$ . Since the current is equal to  $V_d(t)G(t)$ ,  $V_d(t)$  will have its maximum value centered at  $\theta = 0^\circ$  and will therefore be equal to the sum of cosines.

The bias voltage  $V_0$  in Eq. A3 is the same for all of the p-n junctions, when the “GRAYZEL JFET” is biased as described in this paper. There will however, be a variation of the depletion region along the channel due to  $v(t)$ . This variation will be small and is neglected in this analysis.

The amplifier shown in Figure A1 where the FET is a “GRAYZEL JFET” will be analyzed with the aid of the circuit in Figure A2. Voltage  $v(t)$  appears across the RF choke and across the load  $Y(\omega)$  which is in series with blocking capacitor  $C$ .  $V_0+v(t)$  appears across the nonlinear conductance  $G(t)$ . The choke, which is in series with the DC battery, has voltage  $v(t)$  across it but negligible RF current flowing through it. Drain current  $I_d(t) = I_0 + i(t)$  is equal to the product  $G(t)V_d(t)$ . Current  $i(t)$  flows in a loop through the termination  $Y(\omega)$ . DC voltage  $V_0$  appears across the blocking capacitor  $C$ .

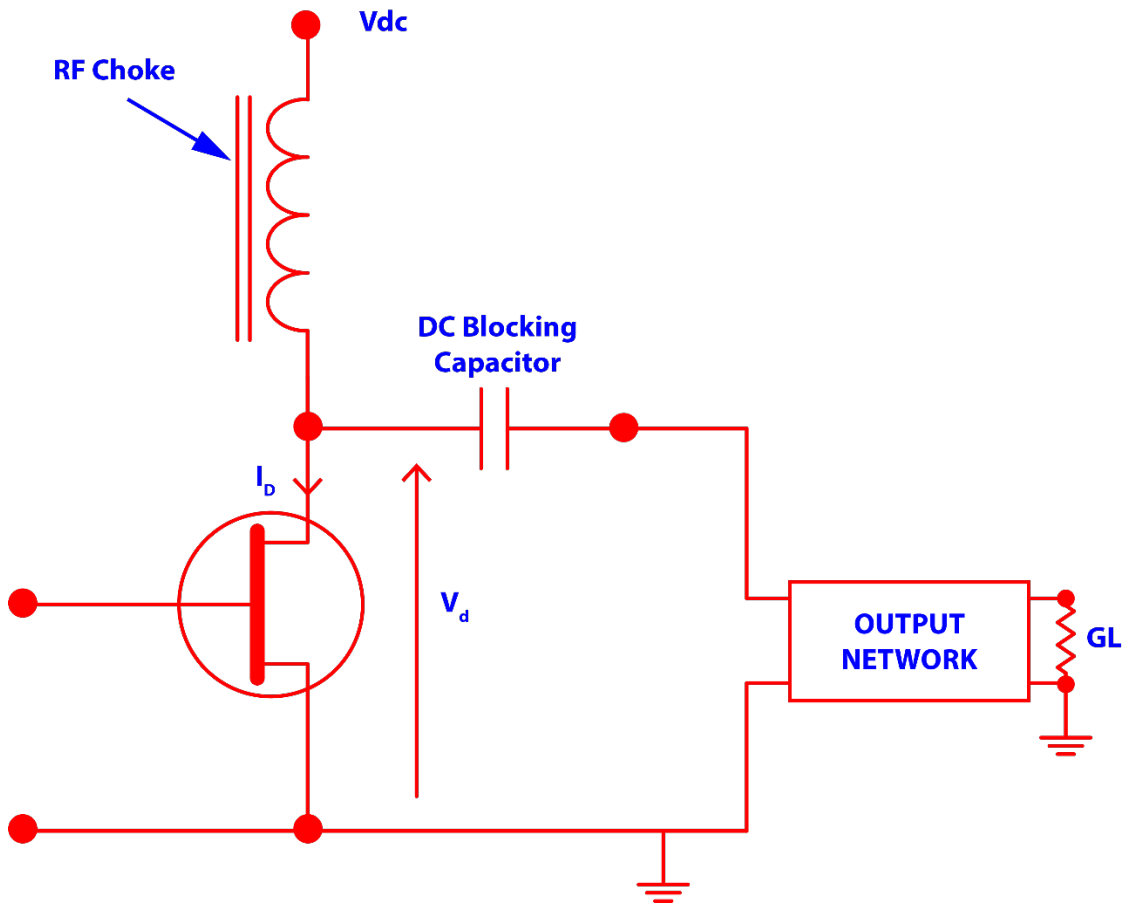


Figure A1. A schematic of a JFET amplifier.

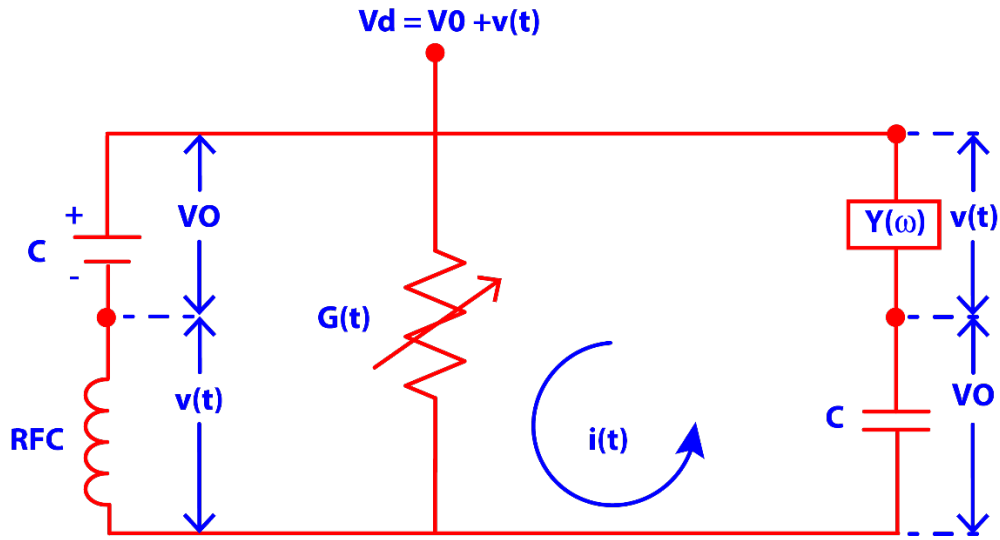


Figure A2. The equivalent circuit of the JFET amplifier shown in Figure A1.

The drain current is given by Eq. A5:

$$\begin{aligned} I_d(t) &= V_d(t)G(t) = [V_0 + v(t)][0.5G_0 + g(t)] \\ &= 0.5V_0G_0 + V_0g(t) + 0.5G_0v(t) + v(t)g(t) \end{aligned} \quad (A5)$$

Eqs. A2, A4 and A5 yield for the terms in Eq. A5

$$V_0g(t) = V_0(2G_0/\pi) (\sum_{k=1}^{\infty} (-1)^{k-1} \text{Cos}((2k-1)\theta) / (2k-1))$$

$$0.5G_0v(t) = 0.5G_0 ( V_1 \text{Cos}(\theta) + \sum_{k=1}^{\infty} V_{2k} \text{Cos}(2k\theta) ) \quad (A5a)$$

$$v(t)g(t) = (2G_0/\pi) [ V_1 \text{Cos}(\theta) + \sum_{k=1}^{\infty} V_{2k} \text{Cos}(2k\theta) ] [ \sum_{j=1}^{\infty} (-1)^{j-1} \text{Cos}((2j-1)\theta) / (2j-1) ]$$

The drain current can be written as the sum of the DC term, the odd harmonics, and the even harmonics:

$$I_d(t) = I_0 + \sum_{k=1}^{\infty} (I_{2k-1}) \text{Cos}(2k-1)\theta + \sum_{k=1}^{\infty} (I_{2k}) \text{Cos}(2k)\theta \quad (A6)$$

Using the identity  $\text{Cos}(x)\text{Cos}(y) = 0.5[\text{Cos}(x+y) + \text{Cos}(x-y)]$ , in Eq. A5a the even harmonics can be written as Eq. A7:

$$I_{2k} = G_0 \{ 0.5V_{2k} - (2V_1/\pi)(-1)^k / (4k^2 - 1) \} \quad (A7)$$

Since the current at the even harmonics is zero, it is possible to solve for voltage  $V_{2k}$  by setting current  $I_{2k}$  equal to zero in Eq. A7, yielding Eq. A8:

$$V_{2k} = (4/\pi)(V_1)(-1)^k / (4k^2 - 1) \quad (A8)$$

Collecting the terms in  $\text{Cos}(\theta)$  in Eq. A5, the value of the current at the fundamental frequency  $I_1$ , is given by Eq. A9:

$$I_1 = G_0[2V_0/\pi + 0.5V_1 -(2/\pi) \sum_{k=1}^{\infty} (-1)^k V_{2k} / (4k^2-1)] \quad (\text{A9})$$

Substituting Eq. (A8) into Eq. (A9) yields Eq. (A10):

$$I_1 = G_0 [2V_0/\pi + V_1 \{0.5 - (8/\pi^2) \sum_{k=1}^{\infty} 1/(4k^2-1)^2\}] \quad (\text{A10})$$

The term  $[0.5 - (8/\pi^2) \sum_{k=1}^{\infty} 1/(4k^2-1)^2]$  was found to converge in the limit to  $(\pi/2)^2$  as  $k$  approaches infinity. (This limit was first estimated and then verified by computer program.) Substituting  $(\pi/2)^2$  for  $[0.5 - (8/\pi^2) \sum_{k=1}^{\infty} 1/(4k^2-1)^2]$  in Eq. A10 yields Eq. A11

$$I_1 = G_0 [2V_0/\pi + (2/\pi)^2 V_1] \quad (\text{A11})$$

At the fundamental frequency  $Y(\omega) = G_L$  and  $I_1 = - (G_L)(V_1)$ . Equating  $I_1$  as given by Eq. A11, to  $- (G_L)(V_1)$ , yields Eq. A12.

$$2G_0V_0/\pi + G_0V_1(2/\pi)^2 = - G_LV_1 = - XG_0V_1 \quad (\text{A12})$$

where  $X = G_L/G_0 = 1/(G_0R_L)$ . Solving Eq. A12 yields Eq. A13:

$$V_1 = - (2/\pi)V_0 / (X + (2/\pi)^2) \quad (\text{A13})$$

The DC current  $I_0$  is found from Eq. A5 to have two terms. The first term is  $0.5(G_0)(V_0)$  and the second DC term results from the product  $(2G_0/\pi)\text{Cos}\theta(V_1\text{Cos}\theta)$ . The DC current is given by Eq. A14.

$$I_0 = .5G_0V_0 + G_0V_1/\pi = 0.5G_0V_0[1 + (2/\pi)/(V_1/V_0)] \quad (\text{A14})$$

Substituting Eq. A13 into Eq. A14 yields:

$$I_0 = 0.5G_0V_0X / (X + (2/\pi)^2) \quad (\text{A15})$$

The DC power is given by A16:

$$P_0 = I_0V_0 = 0.5G_0V_0^2X / (X + (2/\pi)^2) \quad (\text{A16})$$

The output power at the fundamental frequency,  $P_1$ , is found by Eq. A17:

$$P_1 = 0.5G_LV_1^2 = .5G_L[(2/\pi)V_0 / (X + (2/\pi)^2)]^2 \quad (\text{A17})$$

The efficiency (EFF) is then:

$$\text{EFF} = P_1/P_0 = (2/\pi)^2 / [X + (2/\pi)^2] \quad (\text{A18})$$

Figure A3 is a plot of Eq. A18; the efficiency as a function of X.

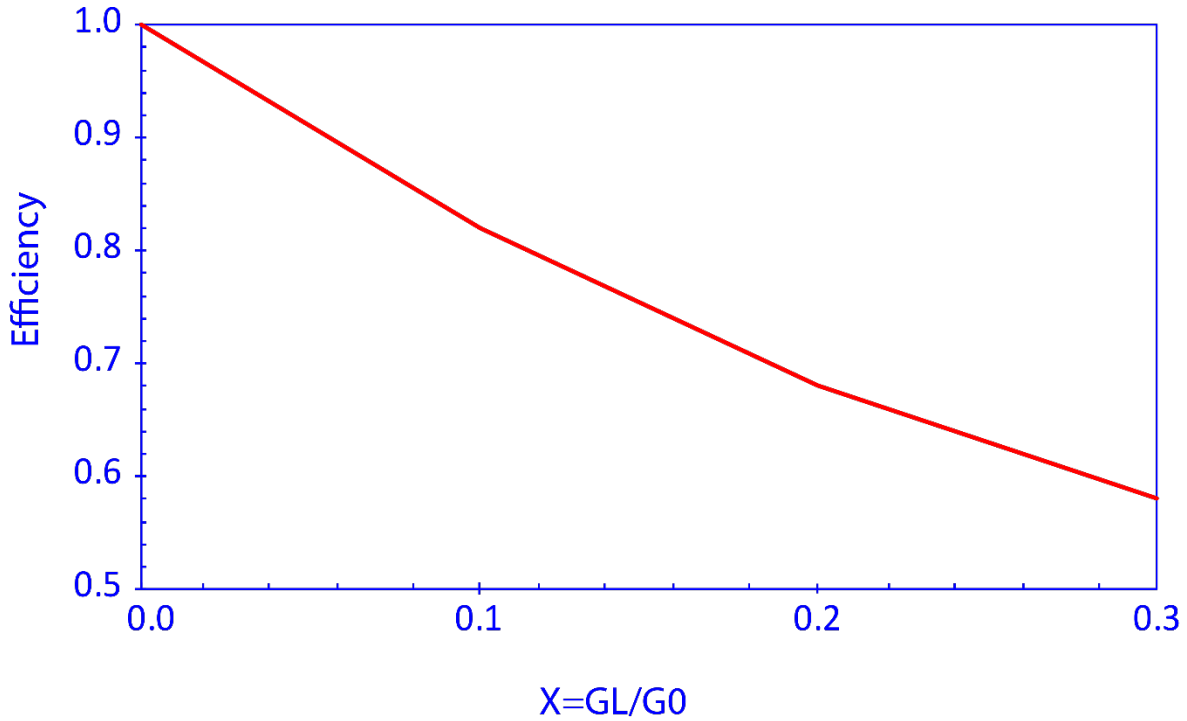


Figure A3. Efficiency as a function X for the “Grayzel JFET” as given by Eq. A18.

The maximum output power is constrained by the condition that the voltage back-biasing the p-n junction must be less than the breakdown voltage  $V_b$ . It can be seen from Eq. A8 that  $V_{2k}$  is proportional to  $V_0$  and from Eq. A13 that  $V_1$  is proportional to  $V_0$ . Eq. A3 and Eq. A4 then yield the result that the drain voltage  $V_d(t)$  is proportional to  $V_0$ . To determine the maximum output power the value of  $V_0$  at breakdown must be determined. Figure A4 shows a typical plot of the drain voltage over one cycle when  $V_0$  equals 1. The maximum voltage occurs at 180 degrees.  $V_{d180}$  the value of  $V_d(t)$  at 180 degrees is given by Eq. A19 where Eq. A4 has been evaluated at 180 degrees.

$$V_{d180} = V_0 - V_1 + \sum_{k=1}^{\infty} V_{2k} \quad (\text{A19})$$

Substituting Eq. A8 and Eq. A13 into Eq. A19 yields Eq. A20.

$$V_{d180} = V_0 \left\{ 1 + [(2/\pi) / (X + (2/\pi)^2)] \left( 1 - 4/\pi \sum_{k=1}^{\infty} (-1)^k / (4k^2 - 1) \right) \right\} = V_0 V_{\text{norm}} \quad (\text{A20})$$

where

$$V_{\text{norm}} = V_{d180} / V_0 \quad (\text{A21})$$



At 180 degrees the JFET is cutoff;  $V_g = V_p$  and for an n-type JFET  $V_p$  is negative.  $V_0$  must therefore satisfy the inequality given by Eq. A22.

$$V_0 < (V_b - |V_p|) / V_{norm} \tag{A22}$$

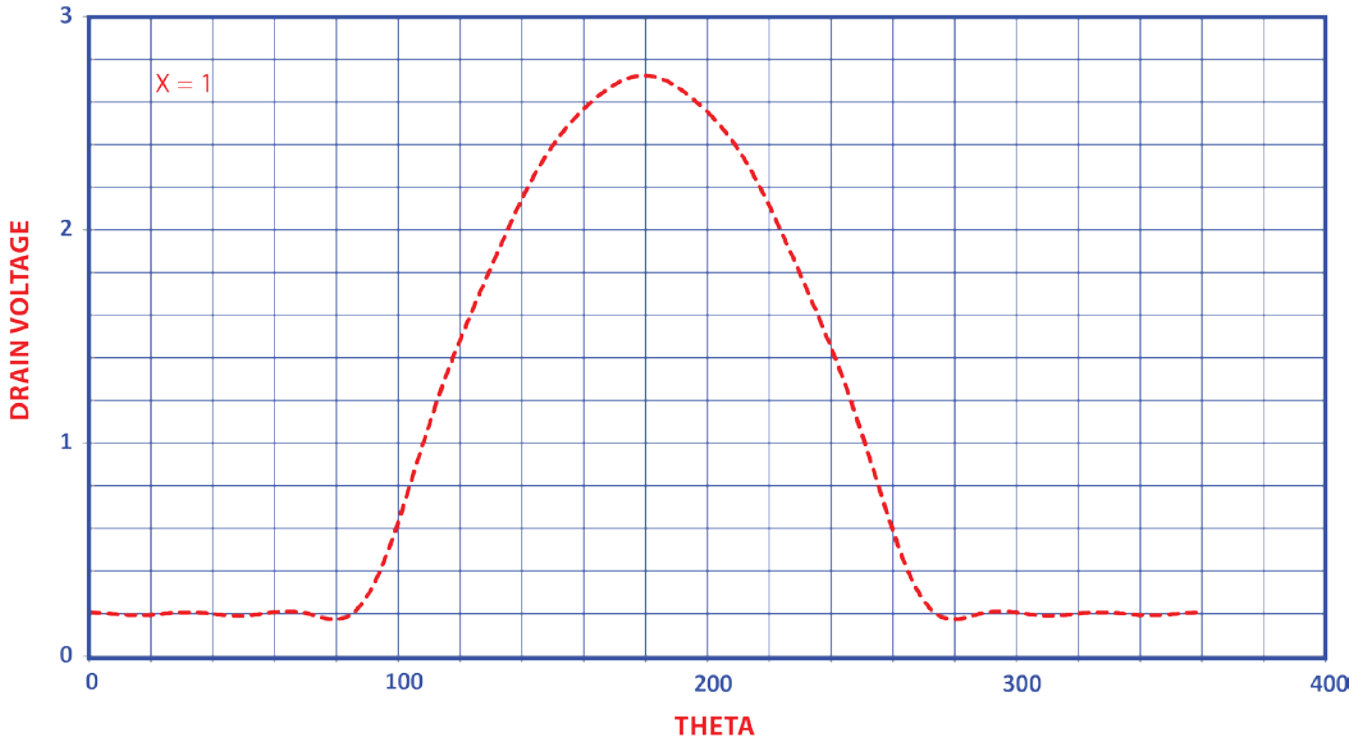


Figure A4. Typical plot of the drain voltage over a cycle where  $V_0$  is equal to one

A plot of Eq. A20 is shown in Fig. A5 where  $V_{d180}$  is plotted as a function of  $X$ . Substituting the maximum value of  $V_0$  given by Eq. A22 into Eq. A17 yields the maximum output power  $P_{1max}$ .

$$P_{1max} < .5G_L[(2/\pi) / (X + (2/\pi)^2)]^2 [(V_b - |V_p|) / V_{norm}]^2 \tag{A23}$$

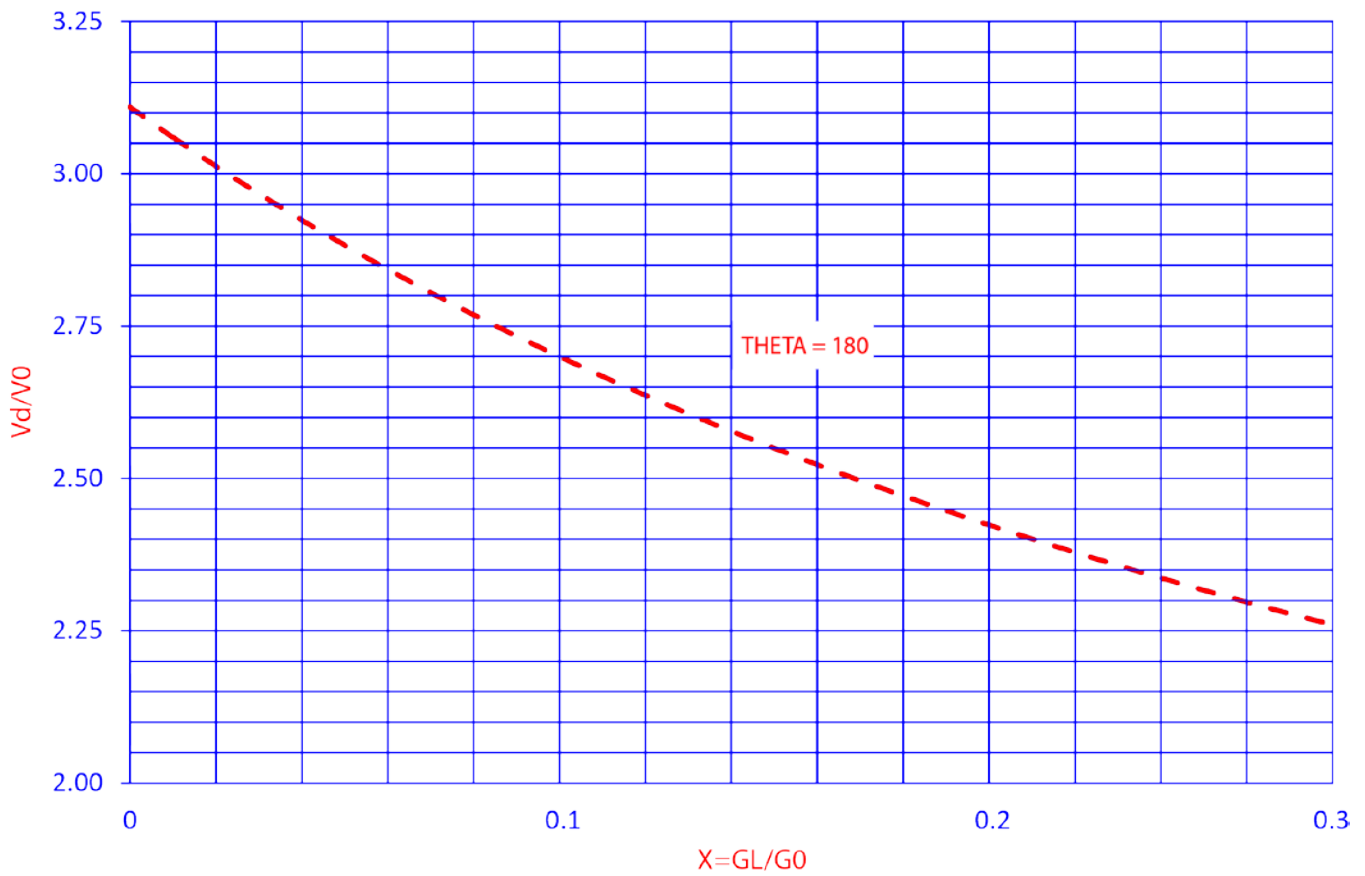


Figure A5.  $V_{d180}$  as a function of  $X$ .

The case where the amplifier is terminated in an open circuit for even harmonics and a short circuit for odd harmonics gives good results; however, it is not necessarily an optimum termination. An analysis similar to that which was performed above but, where the amplifier is terminated in an impedance which presents an open circuit at odd harmonics and a short circuit at even harmonics gave a poorer result. Optimization is required to determine an optimum termination.