REVISIONS						
ZONE REV DESCRIPTION DATE APP						
	-	PRELIMINARY	8/2/19	S. PALACIO		

	NAME:	DATE:
CONTRACT NO:		
DRAWN:	C. Wenner	8/2/19
CHECKED:		
PROJ ENGR:	S. Palacio	8/2/19
PROG MGR:		
MFG.ENGR:		
QA ENGR:	J. Peacher	8/2/19
RELIABILITY:		

Planar Monolithics Industries, Inc. 7311-F GROVE ROAD FREDERICK, MD 21704

ACCEPTANCE TEST PROCEDURE

MODEL: DFD-2G18G-5512



SIZE A	CAGE CODE 05XQ0
SCALE	N/A

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1.0 INTRODUCTION

The DFD-2G18G-5512 provides a digital output representing the frequency of the input RF signal, ranging from 2.0 to 18.0 GHz.

The purpose of this document is to give the necessary information to verify the electrical performance of the DFD-2G18G-5512 Digital Frequency Discriminator (DFD).

2.0 LIST OF TEST EQUIPMENT

- Power Supplies: Minimum 100 mA @ -5 VDC, 2 A @ +5 VDC and 1 A @ +12 VDC are required.
 Sample equipment: Agilent E3634A.
- Signal Generator: Minimum output frequency range from 2.0 GHz to 18.0 GHz and output power level range of -50 dBm to +17 dBm plus maximum cable loss. For example, if maximum cable loss is 1.2 dB, output power level should be at least 18.2 dBm. Sample equipment: Agilent E8257D.
- Noise Source: Broadband noise source with output level of -53 dBm plus maximum cable loss. Sample equipment: Custom noise source unit built around Mercury Systems NS5100-A2X.
- Logic Analyzer or similar Digitizer: Minimum 500 megasample/second digitizing rate and at least 16 channels. Sample equipment: Agilent 1672G.
- Pattern or Function Generator: 50 MHz and 5 Vp-p square wave output capable. Sample equipment: Agilent 33250A.
- Spectrum Analyzer or Network Analyzer or Power Meter: Used for cable loss measurements. Sample equipment: Agilent E4448A.
- Personal Computer: For data acquisition and/or control purposes.



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3.0 ELECTRICAL SPECIFICATIONS

Electrical specifications of DFD-2G18G-5512 are given in Table 1.

Table 1: Electrical Specifications

Frequency Range:		2.0 to 18.0 GHz 16 GHz minimum		
Dynamic Range:		-50 to +15 dBm		
Mean Frequency Resolution:		1 MHz		
Frequency Accuracy:		3 MHz (Peak rms) @ 3 dB SNR *		
Peak Frequency Error:		15 MHz		
Maximum RF Input Power:		+17 dBm CW		
Throughput Tim	ie:	Less than 350 ns typical		
Recovery Time:		50 ns typical		
Shadow Time:		100 ns typical		
Minimum Pulse Width:		100 ns typical		
		-5 VDC @ 30 mA typical		
Power consump	tion:	+5 VDC@ 1.5 A typical		
		+12 VDC @ 800 mA typical		
Control Logic:		14-bit TTL digital output (single ended)		
	RF Input	SMA female		
Connectors:	Power/Control	51-pin micro-D		
	Calibration/Test	15-pin micro-D		



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4.0 ELECTRICAL INTERFACE

Connector allocation information for 51 pin Micro-D and 15 pin Micro-D connectors of DFD-2G18G-5512 are given in Table 2 and Table 3, respectively.

Table 2: 51 Pin Micro-D Connector Allocations

	Po	wer/Contr	ol Pin Out Table		
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	0 V	18	0 V	35	Freq. 13
2	0 V	19	IFM Clock	36	+ 12 V
3	0 V	20	0 V	37	0 V
4	0 V	21	0 V	38	Freq. 0
5	0 V	22	0 V	39	Freq. 2
6	Ext. Trigger**	23	Freq. 1	40	Freq. 4
7	0 V	24	0 V	41	Freq. 5
8	0 V	25	Freq. 3	42	0 V
9	0 V	26	0 V	43	Freq. 7
10	0 V	27	Bad Data	44	Freq. 6
11	0 V	28	0 V	45	0 V
12	0 V	29	Freq. 11	46	Freq. 9
13	Data Valid**	30	0 V	47	Freq. 8
14	0 V	31	Freq. 12	48	Freq. 10
15	0 V	32	0 V	49	0 V
16	0 V	33	0 V	50	+5 V
17	-5 V	34	0 V	51	+5 V



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Table 3: 15 pin Micro-D Connector Allocations

C	alibration/Test		
Pin Out Table			
PIN	SIGNAL		
1	0 V		
2	TDI-PROM		
3	TDO-FPGA		
4	TCK		
5	TMS		
6	VCCO		
7	Test. 17		
8	Test. 18		
9	Test. 19		
10	Test. 20		
11	Test. 21		
12	Test. 22		
13	Sync-In		
14	0 V		
15	Trig-In		



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5.0 FREQUENCY CODING

5.1 IN BAND FREQUENCY CODING

From 1.95 GHz to 18.05 GHz, the frequency code f_N (which is an integer) should be defined as:

 $f_N = INT(f_{in}-1850)$, where f_{in} is the input frequency

5.2 OUT OF BAND FREQUENCY CODING

For signals within the unambiguous bandwidth and outside the defined in-band signals, the following frequency codes should be generated:

 $\begin{array}{ll} f_N = 0 & (1.5 \text{ GHz} < f_{in} < 1.95 \text{ GHz}) \\ f_N = 16383 & (18.05 \text{ GHz} < f_{in} < 18.5 \text{ GHz}) \\ f_N = \text{Undefined} & (f_{in} < 1.5 \text{ GHz} \text{ or } f_{in} > 18.5 \text{ GHz}) \end{array}$

6.0 MEASUREMENT TIMINGS

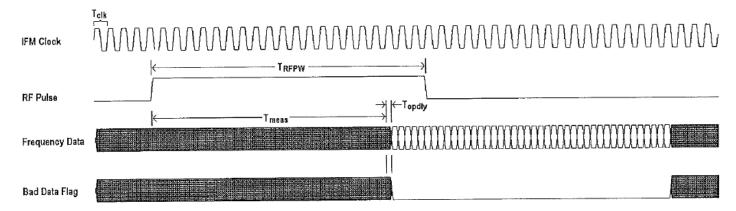


Figure 1: Measurement Cycle

Timing parameters are given in Table 4.

Table 4: Timing Parameters

D .	Description	Timings			
Parameter		Min.	Nominal	Max.	
Tclk	Clock Period	20 ns		100 ns	
T _{RFPW}	RF pulse width	Tclk+80 ns		CW	
T _{meas}	Measurement Time		350 ns		
Topdly	Data output delay	0 ns		10 ns	



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7.0 TESTS

The test setup is shown in Figure 2:

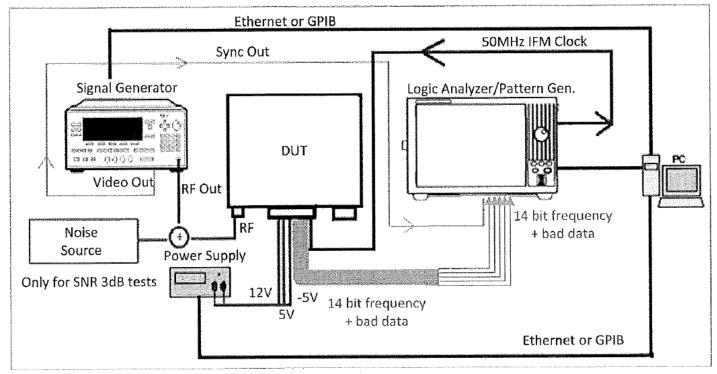


Figure 2: The test setup

7.1 CURRENT TEST

Current limits are as follows:

- -5 V supply current should be between 20 mA and 100 mA
- +5 V supply current should be between 1.3 A and 1.6 A
- +12 V supply current should be between 0.7 A and 1 A

7.2 FREQUENCY SWEEP TEST (HIGH SNR)

- A representative test setup is shown in Figure 2.
- Signal Generator is set to -50 dBm*** output signal level. Pulse Mode is turned on and 100 ns pulse width is set.
- A 50 MHz 0-5 V peak to peak square wave DFD/IFM clock is fed to the DFD.
- Frequency is swept from 2.0 GHz to 18.0 GHz with 1 MHz steps and the frequency data of the DFD (f_N) is read at each frequency****.
- Frequency reading error should be equal to or less than 4.5 MHz* rms.
- Peak frequency reading error should be equal to or less than 15 MHz.



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7.3 FREQUENCY SWEEP TEST (3 dB SNR)

- A noise source with an output of -53 dBm*** is used in the setup given in Figure 2.
- Signal Generator is set to -50 dBm*** output level. Pulse Mode is turned on and 100 ns pulse width is set.
- Frequency is swept from 2.0 GHz to 18.0 GHz with 1 MHz steps and the frequency data of the DFD (f_N) is read at each frequency****.
- RMS Error should be below 4.5 MHz* RMS.
- Peak Error should be below 15 MHz.

7.4 AMPLITUDE SWEEP TEST (HIGH SNR)

- Test setup given in Figure-1 is prepared.
- Signal Generator is set to -50 dBm*** at 10 GHz signal level. Pulse Mode is turned off.
- Sweep amplitude from -50 dBm*** to 10 dBm*** with 10 dBm steps and read the frequency data of the DFD at each amplitude level.
- Frequency reading error should be equal to or less than 4.5 MHz* rms.
- Peak frequency reading error should be equal to or less than 15 MHz.
- *To increase the production yield, DFD's rms frequency accuracy limit is set to 4.5 MHz for standard productions tests, which is satisfactory for most system specifications they are used in. For most DFDs actual rms frequency accuracy results are lower than 3 MHz.
- **Connector pins 6 and 13 are reserved for External Trigger feature.
- ***Cable losses should be included.
- ****The frequency reading f_N of the DFD should be preferably fed to an algorithm to filter some of the erroneous readings.



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