REVISIONS						
ZONE	REV	DESCRIPTION	DATE	APPROVED		
	-	PRELIMINARY	8/2/19	S. PALACIO		

	NAME:	DATE:
CONTRACT NO:		
DRAWN:	C. Wenner	8/2/19
CHECKED:		
PROJ ENGR:	S. Palacio	8/2/19
PROG MGR:		
MFG.ENGR:		
QA ENGR:	J. Peacher	8/2/19
RELIABILITY:		

Planar Monolithics Industries, Inc. 7311-F GROVE ROAD FREDERICK, MD 21704

OPERATING MANUAL

MODEL: DFD-2G18G-5512



SIZE A	CAGE CODE 05XQ0
SCALE	N/A

DWG. NO. **PRELIMINARY**

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TABLE OF REVISIONS

DESCRIPTION	DATE	PMI
PRELIMINARY	8/2/19	S. PALACIO



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1.0 INTRODUCTION The purpose of this document is to give the necessary information to be able to use the DFD-2G18G-5512 Digital Frequency Discriminator (DFD). The DFD-2G18G-5512 provides a digital output representing the frequency of the input RF signal, ranging from 2.0 to 18.0 GHz. DFD-2G18G-5512 is a clocked sampling DFD which samples the RF input on the rising edge of every master clock cycle and provides a digital output accordingly. CAGE



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2.0 GLOSSARY

CW: Continuous Wave dBm: Decibel milliWatt

DFD: Digital Frequency Discriminator rms: root mean square SNR: Signal to Noise Ratio



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3.0 ELECTRICAL SPECIFICATIONS

Electrical specifications of DFD-2G18G-5512 are given in Table 1.

Table 1: Electrical Specifications

Frequency Range:		2.0 to 18.0 GHz 16 GHz minimum		
Dynamic Range:		-50 to +15 dBm		
Mean Frequency Resolution:		1 MHz		
Frequency Accura	ncy:	3 MHz (Peak rms) @ 3 dB SNR		
Peak Frequency E	rror:	15 MHz		
Maximum RF Inp	ut Power:	+17 dBm CW		
Througoutput Tim	ne:	Less than 350 ns typical		
Recovery Time:		50 ns typical		
Shadow Time:		100 ns typical		
Minimum Pulse V	Vidth:	100 ns typical		
		-5 VDC @ 30 mA typical		
Power consumption	on:	+5 VDC@ 1.5 A typical		
_		+12 VDC @ 800 mA typical		
Control Logic:		14-bit TTL digital output (single ended)		
	RF Input	SMA female		
Connectors:	Power/Control	51-pin micro-D		
	Calibration/Test	15-pin micro-D		



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4.0 ELECTRICAL INTERFACE

Connector allocation information for 51 pin Micro-D and 15 pin Micro-D connectors of DFD-2G18G-5512 are given in Table 2 and Table 3, respectively.

Table 2: 51 Pin Micro-D Connector Allocations

POWER/CONTROL PIN OUT TABLE						
PIN	N SIGNAL		SIGNAL	PIN	SIGNAL	
1	0 V	18	0 V	35	Freq. 13	
2	0 V	19	IFM Clock	36	+ 12 V	
3	0 V	20	0 V	37	0 V	
4	0 V	21	0 V	38	Freq. 0	
5	0 V	22	0 V	39	Freq. 2	
6	Ext. Trigger*	23	Freq. 1	40	Freq. 4	
7	0 V	24	0 V	41	Freq. 5	
8	0 V	25	Freq. 3	42	0 V	
9	0 V	26	0 V	43	Freq. 7	
10	0 V	27	Bad Data	44	Freq. 6	
11	0 V	28	0 V	45	0 V	
12	0 V	29	Freq. 11	46	Freq. 9	
13	Data Valid*	30	0 V	47	Freq. 8	
14	0 V	31	Freq. 12	48	Freq. 10	
15	0 V	32	0 V	49	0 V	
16	0 V	33	0 V	50	+5 V	
17	-5 V	34	0 V	51	+5 V	

^{*}Connector pins 6 and 13 are reserved for future use.

Table 3: 15 pin Micro-D Connector Allocations

CALIBRATION/TEST						
PIN OUT TABLE						
PIN	SIGNAL					
1	0 V					
2	TDI-PROM					
3	TDO-FPGA					
4	TCK					
5	TMS					
6	VCCO					
7	Test. 17					
8	Test. 18					
9	Test. 19					
10	Test. 20					
11	Test. 21					
12	Test. 22					
13	Sync-In					
14	0 V					
15	Trig-In					



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5.0 TYPICAL CONNECTION DIAGRAM

Typical connection diagram is shown below:

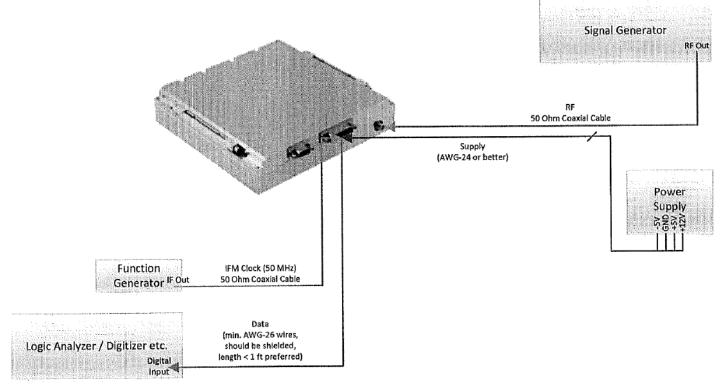


Figure 1: Typical Connection Diagram

6.0 FREQUENCY CODING

6.1 IN BAND FREQUENCY CODING

From 1.95 GHz to 18.05 GHz, the frequency code f_N (which is an integer) should be defined as:

 $f_N = INT(f_{in}-1850)$, where f_{in} is the input frequency

6.2 OUT OF BAND FREQUENCY CODING

For signals within the unambiguous bandwidth and outside the defined in-band signals, the following frequency codes should be generated.

 $\begin{array}{ll} f_N = 0 & (1.5 \text{ GHz} < f_{in} < 1.95 \text{ GHz}) \\ f_N = 16383 & (18.05 \text{ GHz} < f_{in} < 18.5 \text{ GHz}) \\ f_N = \text{undefined} & (f_{in} < 1.5 \text{ GHz} \text{ or } f_{in} > 18.5 \text{ GHz}) \end{array}$



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7.0 MEASUREMENT TIMINGS

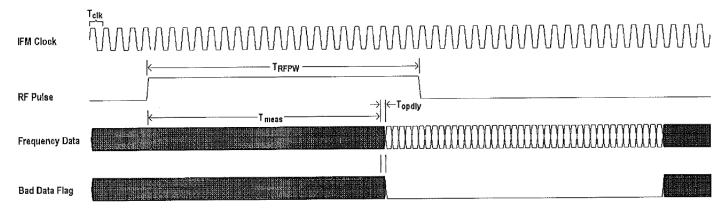


Figure 2: Measurement Cycle

Timing parameters are given in Table 4.

Table 4: Timing Parameters

D	Description	Timings			
Parameter		Min.	Nominal	Max.	
Telk	Clock Period	20 ns		100 ns	
TRFPW	RF pulse width	Tclk+80 ns		CW	
Tmeas	Measurement Time		350 ns		
Topdly	Data output delay	0 ns		10 ns	



SIZE A	CAGE CODE 05XQ0
SCALE	N/A

8.0 MECHANICAL SPECIFICATIONS

8.1 DIMENSIONS

152 mm x 147 mm x 32.5 mm 5.98" x 5.79" x 1.28"

8.2 WEIGHT

The typical weight is 1.15 kg.

8.3 COOLING

Natural convection and radiation

8.3 SERVICEABILITY

The module is sealed and not user serviceable.

9.0 ENVIRONMENTAL SPECIFICATIONS

Temperature: -40°C to +60°C (Operating)

-55°C to +95°C (Storage)

Humidity: MIL-STD-202, Method 103B Cond. B Shock: MIL-STD-202, Method 213B Cond. B Vibration: MIL-STD-202, Method 204D Cond. B Altitude: MIL-STD-202, Method 105C Cond. A Temperature Cycle: MIL-STD-202, Method 107G Cond. A



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