



Features and Benefits

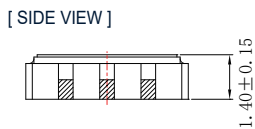
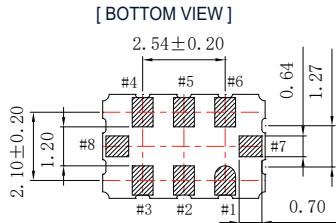
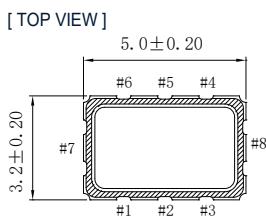
- Low Power Supply Voltage: 3.3, 2.5, 1.8V supply options
- Clock Output: CMUU
- Output frequency support from 15MHz to 250MHz
- Ultra Low Noise, Phase Jitter < 300 fs
(Typical: 150 fs at 12kHz to 20MHz frequency offsets)
- Tri-state enable / disable mode.
- Temperature Range: -40°C to +85°C
- Pb-free/RoHS Compliant

Typical Applications

- SONET/SDH, Gigabit Ethernet.
- Storage Area Networking (SAN)
- SD/HD video
- FPGA clock generation

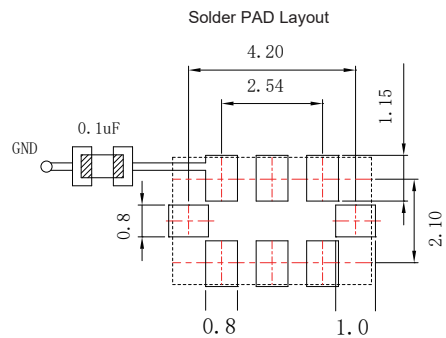
Mechanical Drawing & Pin Connections

Drawing No: MD200027-&



PIN#	FUNCTION
	CMOS
1	NC
2	OE
3	GND
4	Output
5	NC
6	VDD
7	NC
8	NC

Unit in mm
 1mm = 0.0394 inches





Specifications

Specification	Condition	3.3V		2.5V		1.8V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation	V _{DD} ±5%	-	-	-	-	1.71	1.89	V
Supply Voltage Variation	V _{DD} ±10%	3.63	2.97	2.25	2.75	-	-	V
Frequency Range		15	250	15	250	15	250	MHz
Standard Frequency		100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400, 491.52, 622.08, 644.531250						MHz
Supply Current		-	90	-	80	-	70	mA
Duty Cycle	F<100MHz	45	55	45	55	45	55	%
	F>100MHz	40	60	40	60	40	60	%
Output Level	Output High	0.9xV _{DD}	-	0.9xV _{DD}	-	0.9xV _{DD}	-	V
	Output Low	-	0.1xV _{DD}	-	0.1xV _{DD}	-	0.1xV _{DD}	
Transition Rise/Fall Time	20%-80%	-	1.2	-	1.5	-	2.0	nSec
Start Time		-	8	-	8	-	8	mSec
Tri-State(Input to Pin2)	Enable	0.7xV _{DD}	-	0.7xV _{DD}	-	0.7xV _{DD}	-	V
	Disable	-	0.3x V _{DD}	-	0.3xV _{DD}	-	0.3xV _{DD}	
Period Jitter		-	100	-	100	-	100	ps

Frequency Stability vs. Temperature

	±20PPM	±25PPM	±30PPM	±50PPM
-20°C to +70°C	Conditional	Available	Available	Available
-40°C to +85°C	Not Available	Conditional	Available	Available

Note: Inclusive of calibration @25°C, operating temperature range, input voltage variation, load variation, aging (1st year), shock and vibration.