Linearity of the JFET and MOSFET when in Saturation over the Entire Cycle

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***Abstract*—It is shown in this letter that for an FET with "hard saturation", the drain current is a linear function of the gate voltage when the gate voltage is sinusoidal and the drain voltage is greater than the saturation voltage over the entire cycle. An FET with "hard saturation" is an FET that has a nearly constant value of drain current when the drain voltage is greater than the saturation voltage When the FET is in saturation over the entire cycle the drain current I_{dsat} is a quadratic function of the gate voltage. Since there are no third order or higher terms there are no third order or higher intermodulation products and the amplifier is therefore linear. When the FET is in saturation over the entire cycle and there is "hard saturation" the drain current is only a function of the gate voltage and the harmonic terminations do not affect the efficiency or the output power, The load impedance should therefore, present a short-circuit at all of the harmonic frequencies, as a harmonic voltage may reduce the drain voltage such that the FET is not in saturation, or increase the drain voltage to a value that will cause breakdown. The required value of resistance as a function of the DC bias voltage and expressions for the maximum power and efficiency are given.**

***Index Terms*— Amplifiers, FET, JFET, MOSFET, pinchoff, p-n junctions**

I. Introduction

As stated in [1] "Performing RF amplification in a way that is simultaneously linear and efficient has long been a challenge in power amplifier (PA) design. In short single-transistor PAs can either be operated in a linear (but inefficient) current source mode of operation or as efficient (but nonlinear) switches, but these two modes are mutually exclusive." In prior art two or more amplifiers are utilized as in the architecture of the "out-phasing technique" [1], or in the architecture of the predistortion linearizing technique [2] or in the architecture of the Dougherty Amplifier [3]. These techniques do not achieve linear amplification but are a compromise between linearity and efficiency. These techniques all use two FETs. This paper demonstrates that linear amplification can be achieved at high power with an efficiency greater than 60%, using a single FET. The "Grayzel Linear Amplifier" (patent pending) utilizes:

1. FETs with "hard saturation" where a "hard saturation" FET has a nearly constant drain current when the drain voltage is greater than V_{dsat} where V_{dsat} is the value of the drain voltage where the drain current first saturates when the gate voltage is at its maximum value.
2. Combinations of bias voltage and load resistance such that the drain voltage is greater than V_{dsat} and less than Vb, the breakdown voltage of the FET over the entire cycle.
3. Impedance transforming networks which present a load resistance which maintains the drain voltage greater than V_{dsat} over the entire cycle.

II. Analysis

A. The JFET

When the drain voltage is less than the pinchoff voltage the drain current of an n type JFET is given Eq. 1 [4].

$$I_{ds} = G0\{V_{dsat} - 2/3(V_{bi}- Vp) [1 - ((V_{bi}-Vg)/(V_{bi}-Vp))^{3/2}]\} \quad (1)$$

where G0 is the conductance of the channel when there is no depletion layer, Vg is the gate voltage, Vp is the pinchoff voltage, and V_{bi} is the "built in" p-n junction potential. When the drain voltage is greater than $V_{dsat,}$ the drain current I_{ds} is solely a function of the gate voltage and a very good approximation for the drain current is given Eq. 2 [4], where I_{dss} is the value of the saturated drain current when Vg=0.

$$I_{ds} = I_{dss}(1-Vg/Vp)^2 \quad (2)$$

For an n type JFET, when the gate voltage is given by Eq. 3 and K=1, the gate voltage has a maximum of zero and a minimum of Vp, where Vp is negative. For K<1 the gate voltage is a cosine wave without any clipping.

$$Vg = (Vp/2)(1 - K\,Cos(\omega t)) \quad (3)$$

Substituting Eq. 3 into Eq. 2 yields Eq. 4

$$I_{ds} / I_{dss} = (2+K^2)/8 +(1/2)KCos(\omega t)+(K^2/8)Cos(2\omega t)) \quad (4)$$

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The component of the drain voltage at the fundamental frequency is given by Eq. 5, where R_{in} is the resistance presented between the drain and the source.

$$V_{drain} = -K\,(1/2)\mathrm{Cos}(\omega t)\,R_{in} \quad (5)$$

The minus sign is required since the drain current flows in a loop from the drain to the source and through the load resistor to the drain.

It can be seen from Eq. 3 and Eq. 5 that for $K \leq 1$ that when the gate voltage is a sinusoid proportional to K, the drain voltage is a sinusoid proportional to K and the amplifier is linear.

B. The MOSFET

There are two theories for obtaining a relationship for the drain current as a function of the gate voltage for the MOSFET, when the drain voltage is greater than or equal to the V_{dsat}; the square law theory and the bulk charge theory. In the following analysis the square law theory will be used as it is simpler and gives good insight into the performance of the MOSFET.

According to the square law theory; when the drain voltage is greater than or equal to V_{dsat} , I_{dsat} is given by Eq. 6,

$$I_{dsat} = (Z\mu'_nC_0/2L)(V_g - V_T)^2 \quad (6)$$

where, $\mu'_n$is the average mobility of the inversion layer carriers, C_0 is the oxide capacitance, Z is the width of the channel, L is the length of the channel and V_T is the threshold voltage [5].

When the gate voltage is given by Eq. 7,

$$V_g = (V_{gmax} + V_T)/2 + K\,[\,(V_{gmax} - V_T)/2]\,\mathrm{Cos}(\omega t) \quad (7)$$

where V_{gmax} is the maximum gate voltage. When K=1 V_g has a maximum value of V_{gmax} and a minimum value of V_T. Substituting Eq. 7 into Eq. 6 yields Eq. 8.

$$I_{dsat} = (Z\mu'_nC_0/2L)[(V_{gmax} - V_T)^2\,(1 + K\mathrm{Cos}(\omega t))/2]^2 \quad (8)$$

I_{dss}, the saturated drain current when V_g is equal to V_{gmax} is found by setting V_g equal to V_{gmax} in Eq. 6, yielding Eq. 9.

$$I_{dss} = (Z\mu'_nC_0/2L)(V_{gmax} - V_T)^2 \quad (9)$$

Dividing Eq. 8 by Eq. 9 yields Eq. 10.

$$I_{dsat}/I_{dss} = [\,(1 + K\mathrm{Cos}(\omega t))/2]^2 = (2+K^2)/8 + (1/2)K\mathrm{Cos}(\omega t) + (K^2/8)\mathrm{Cos}(2\omega t) \quad (10)$$

The component of the drain voltage at the fundamental frequency is given by Eq. 11, where R_{in} is the resistance presented between the drain and the source.

$$V_{drain} = -K\,(1/2)\mathrm{Cos}(\omega t)\,R_{in} \quad (11)$$

It can be seen from Eq. 7 and Eq. 11 that for $K \leq 1$ that when the gate voltage is a sinusoid proportional to K, the drain voltage is a sinusoid proportional to K and the amplifier is linear.

It is interesting to observe that Eq. 5 and Eq. 10 are identical; that the JFET and MOSFET yield the same expression for I_{dsat}/I_{dss}.

It is shown in [6] that using the bulk theory one finds that V_{dsat} and I_{dss} differ slightly from the square law analysis but I_{dsat}/I_{dss} is virtually the same.

When the FET is in saturation over the entire cycle it can be seen from Eq. 2 and from Eq. 6 that the drain current I_{dsat} is a quadratic function of the gate voltage. Since there are no third order or higher terms there are no third order or higher intermodulation products. Eq. 2 and Eq. 6 however, only apply to FETs with "hard saturation" where a "hard saturation" FET has a nearly constant drain current when the FET is in saturation. If the FET is not in saturation or the FET does not have "hard saturation" the drain current is a function of both the gate voltage and the drain voltage, and the amplifier is not linear.

When K=1, Eq. 10 yields a DC current equal to $(3/8)I_{dss}$ and a current at the fundamental frequency equal to $I_{dss}/2$. The DC power is then given by Eq. 12,

$$P_0 = (3/8)I_{dss}V_0 \quad (12)$$

where V_0 is the DC bias voltage' The output power at the fundamental frequency P_1, is given by Eq. 13.

$$P_1 = (I_{dss})^2\,R_{in}/8 \quad (13)$$

When the FET is in saturation over the entire cycle and there is "hard saturation" the drain current is not a function of the load impedance. Since only the fundamental frequency is desired at the output, the load impedance should present a short-circuit at all of the harmonic frequencies, as a harmonic voltage may reduce the drain voltage such that the FET is not in saturation, or increase the drain voltage to a value that will cause breakdown. For an n type JFET the saturation voltage is equal to $(V_g - V_p)$ [4] and V_{dsat} the saturation voltage when Vg equals zero equals |Vp|. For a MOSFET the saturation voltage is equal to $(V_g - V_T)$ [5] and V_{dsat} the saturation voltage when Vg equals V_{gmax} is equal to $V_{gmax} - V_T$. For a given value of V_0, when the load impedance presents a short-circuit at all of the harmonic frequencies, the constraint that the FET is in saturation over the entire cycle requires that for the JFET, the amplitude of the fundamental frequency has a maximum value of $V_0 - |V_p|$ and that for the MOSFET the amplitude of the fundamental frequency has a maximum value of $V_0 - (V_{gmax} - V_T)$. The minimum value of the drain voltage is then equal to $V_{dsat.}$ Since the drain current flowing through the load resistor is sinusoidal and has a value $I_{dss}/2$, the load resistance is given by Eq. 14a for the JFET and Eq. 14b for the MOSFET.

$$Rin = (V_0 - |Vp|)/(I_{dss}/2) \quad (14a)$$

$$R_{in} = (V_0 - (V_{gmax} - V_T)|) /(I_{dss}/2) \quad (14b)$$

Solving Eq. 14a and 14b for V_0, yields Eq. 15a for the JFET and Eq. 15b for the MOSFET.

$$V_0 = (I_{dss}/2) Rin + |Vp| \quad (15a)$$

$$V_0 = (I_{dss}/2) R_{in} + (V_{gmax} - V_T) \quad (15b)$$

Substituting Eq. 14a and Eq. 14b into Eq. 13 yields the output power at fundamental-frequency, P_1, given by Eq. 16a for the JFET and Eq. 16b for the MOSFET.

$$P_1= (I_{dss}) (V0-|Vp|)/4 \quad (16a)$$

$$P_1= (I_{dss}) (V_0 - (V_{gmax} - V_T))/4 \quad (16b)$$

The efficiency is given by Eq. 17a for the JFET and Eq. 17b for the MOSFET.

$$Eff =P_1 /P_0 = EFF0(V_0 –|Vp|)/V_0 = 2/3(1– |Vp|)/V_0) \quad (17a)$$

$$Eff =P_1 /P_0 = EFF0(V_0 – (V_{gmax} - V_T))/V_0 = 2/3(1 – (V_{gmax} - V_T))/V_0) \quad (17b)$$

where EFF0 is equal to $I_1/2I_0 = 2/3$ for both the JFET and for the MOSFET. It is shown in [6] that analysis using the bulk charge theory gives virtually the same value of EFF0.

For a given value of R_{in} Eq. 15a in the case of a JFET and Eq. 15b in the case of a MOSFET gives the minimum value of V_0 for the condition that the drain voltage is greater than or equal to V_{dsat} over the entire cycle. Increasing V_0 does not increase P_1 since the drain current is saturated but does increase P_0 and therefore decreases the efficiency. Thus, for a given value of R_{in}, the value of V_0 given by Eq. 15a or Eq. 15b yields the highest efficiency. It can be seen from Eq. 17a and Eq. 17b that the efficiency increases with increasing V_0 subject to the constraint that R_{in} is given by Eq. 14a or Eq. 14b.Thus to increase the efficiency both V_0 and R_{in} must be increased. The maximum value of the drain voltage for the JFET, $2V_0 – |Vp|$, and the maximum value of the drain voltage for the MOSFET, $2V_0 – (V_{gmax} - V_T)$, must not exceed the breakdown voltage Vb. V_0 must therefore satisfy Eq. 18a for the JFET and Eq. 18b for the MOSFET.

$$V_0 \leq (Vb + |Vp|)/2 \quad (18a)$$

$$V_0 \leq (Vb + (V_{gmax} - V_T))/2 \quad (18b)$$

Substituting Eq.18a into Eq. 14a and Eq.18b into Eq. 14b yields the inequalities of Eq. 19a for the JFET and Eq. 19b for the MOSFET.

$$R_{in} \leq (2Vb - |Vp|)/I_{dss} \quad (19a)$$

$$R_{in} \leq (2Vb - (V_{gmax} - V_T))/I_{dss} \quad (19b)$$

Substituting Eq. 18a into Eq. 16a and substituting Eq. 18b into Eq. 16b yields the inequality given in Eq. 20a for the JFET and the inequality given in Eq. 20b for the MOSFET.

$$P_1 \leq (I_{dss})(2Vb - |Vp|)/8 \quad (20a)$$

$$P_1 \leq (I_{dss})(2Vb - (V_{gmax} - V_T))/8 \quad (20b)$$

III. Conclusion

When the drain voltage of a “hard saturation” FET is greater than V_{dsat} over the entire cycle and the gate voltage is sinusoidal the output voltage is only a function of the gate voltage and is a linear function of the gate voltage. If the drain voltage is less than V_{dsat} over part of the cycle the output voltage will be a function of both the gate and the drain voltage and will not be a linear function of the gate voltage. To maintain the drain voltage greater than V_{dsat} over the entire cycle, at maximum efficiency, the output circuit must present to the output of a JFET, R_{in} satisfying Eq. 14a with the equal sign and Eq. 14b for a MOSFET and V0 should satisfy Eq, 15a for a JFET and Eq. 15b for a MOSFET and the harmonics should be shorted to ground. For maximum efficiency and maximum power, the output circuit must present to the output of a JFET, R_{in} satisfying Eq. 19a with the equal sign and Eq. 19b for a MOSFET and V0 should satisfy Eq, 15a for a JFET and Eq. 15b for a MOSFET.

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V. References

[1] T. Barton “Not Just a Phase”, IEEE Microwave Magazine Vol. 17 No. 2 February 2016 pp. 18- 31.
[2] Katz, J. Wood, D. Chokola, “The Evolution of PA Linearization”, IEEE Microwave Magazine Vol. 17 No. 2 February 2016 pp. 32- 40.
[3] R. Pengelly, C. Fager, M. Ozen, “Doherty’s Legacy”, IEEE Microwave Magazine Vol. 17 No. 2 February 2016 pp. 41- 57.
[4] R. F. Pierret, Semiconductor Device Fundamentals, Pearson Education Noida, India, 2006, page 540.
[5] Ibid pp. 623.
[6] Grayzel, “A Non-Linear Analysis of the Saturated MOSFET”, High Frequency Electronics, June 2018, pp 22-28 (available at, pmi-rf.com/tech-papers.htm).