



**SUMMARY TEST DATA
ON
P4T-6G18G-27-T-SFF**

PL22281/1810

Customer: _____ Tested By: A. Lopez
 SO No: _____ Temperature: +25°C
 Model No: P4T-6G18G-27-T-SFF Date: 03/08/18
 Serial No: PL22281/1810 Drawing No: 27633410 Rev: A1

TEST. ITEM NO	PARAMETERS	SPECIFIED VALUE	TEST RESULTS	QA QC																																																																		
1	Frequency Range:	6.0 TO 18.0 GHz	6.0 TO 18.0 GHz (See Plots)	PMI QA 2																																																																		
2	Insertion Loss	2.5 dB MAX @ 6.0 GHz TO 8.0 GHz 3.7 dB MAX @ 8.0 GHz TO 12.4 GHz 4.8 dB MAX @ 12.4 GHz TO 18.0 GHz	2.44 dB MAX @ 6.0 GHz TO 8.0 GHz 3.05 dB MAX @ 8.0 GHz TO 12.4 GHz 4.37 dB MAX @ 12.4 GHz TO 18.0 GHz (See Plots)																																																																			
3	Isolation (On/All Ports Off)	45 dB MIN @ 6.0 GHz TO 8.0 GHz 27 dB MIN @ 8.0 GHz TO 18.0 GHz	50.71 dB MIN 53.18 dB MAX (See Plots)																																																																			
4	VSWR	2.3:1 MAX @ 6.0 GHz TO 12.4 GHz 2.0:1 MAX @ 12.4 GHz TO 18.0 GHz	1.81 : 1 (See Plots)																																																																			
5	RF Impedance:	50 Ω	50 Ω																																																																			
6	Switching Speed (ON/OFF):	500 ns MAX (FROM 50% TTL TO 90%/10% RF VOLTAGE)	Switching Speed (ON) 50 ns Switching Speed (OFF) 25 ns (See Typical Characteristics)																																																																			
7	Power Supply:	+5.0 VDC ±5% @ 100 mA MAX -15.0 VDC ±5% @ 60 mA MAX	+5.0 VDC ±5% @ 97 mA -15.0 VDC ±5% @ 30 mA																																																																			
8	Control Logic	LOGIC "0" = -0.3 V TO +0.8 V FOR PORT ON (LOW LOSS STATE) LOGIC "1" = +2.0 V TO +5.0 V FOR PORT OFF (ISOLATION STATE) <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="8">LOGIC TABLE (J1: COMMON PORT)</th> </tr> <tr> <th rowspan="2">PORT</th> <th colspan="4">TTL INPUT LEVEL</th> <th rowspan="2">J1-J2</th> <th rowspan="2">J1-J3</th> <th rowspan="2">J1-J5</th> <th rowspan="2">J1-J6</th> </tr> <tr> <th>E2</th> <th>E3</th> <th>E5</th> <th>E6</th> </tr> </thead> <tbody> <tr> <td>J2</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>ISOLATION LOSS</td> <td>ISOLATION</td> <td>ISOLATION</td> <td>ISOLATION</td> </tr> <tr> <td>J3</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>ISOLATION</td> <td>ISOLATION LOSS</td> <td>ISOLATION</td> <td>ISOLATION</td> </tr> <tr> <td>J5</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>ISOLATION</td> <td>ISOLATION</td> <td>ISOLATION LOSS</td> <td>ISOLATION</td> </tr> <tr> <td>J6</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>ISOLATION</td> <td>ISOLATION</td> <td>ISOLATION</td> <td>ISOLATION LOSS</td> </tr> <tr> <td>ALL OFF</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td colspan="4">ISOLATION</td> </tr> </tbody> </table>	LOGIC TABLE (J1: COMMON PORT)								PORT	TTL INPUT LEVEL				J1-J2	J1-J3	J1-J5	J1-J6	E2	E3	E5	E6	J2	0	1	1	1	ISOLATION LOSS	ISOLATION	ISOLATION	ISOLATION	J3	1	0	1	1	ISOLATION	ISOLATION LOSS	ISOLATION	ISOLATION	J5	1	1	0	1	ISOLATION	ISOLATION	ISOLATION LOSS	ISOLATION	J6	1	1	1	0	ISOLATION	ISOLATION	ISOLATION	ISOLATION LOSS	ALL OFF	1	1	1	1	ISOLATION				Pass	PMI QA 2
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*: 1 μs MAXIMUM PULSE WIDTH
 ²: A UNIT LOAD IS 2.0 mA SINK CURRENT AND 50 μA SOURCE CURRENT

QA/QC Approval:  PMI QA 2 Date: 3/8/18

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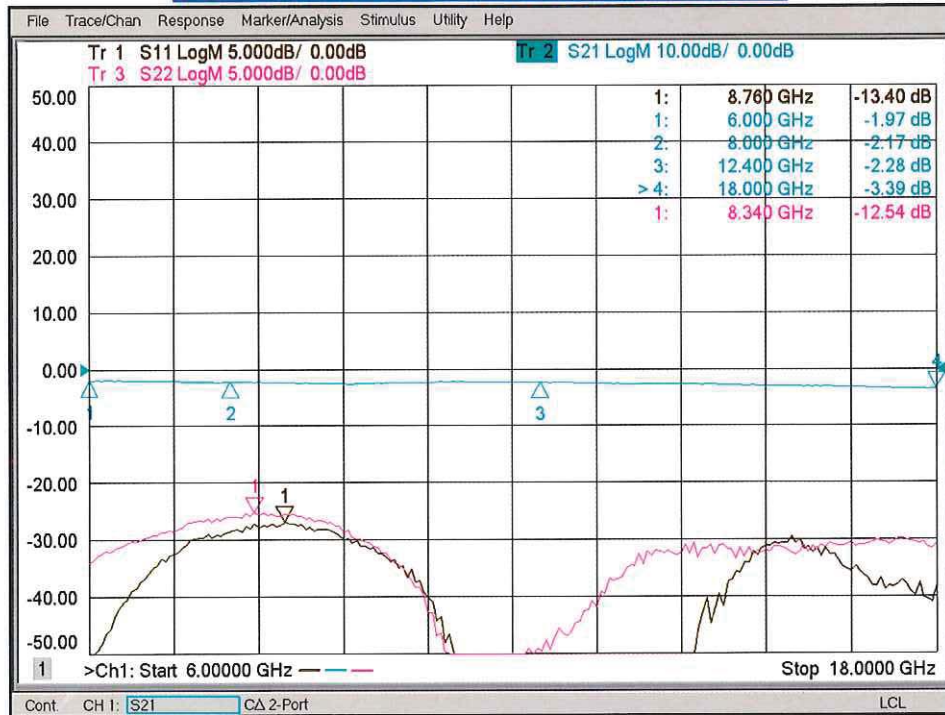
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(J1 – J2) Insertion Loss and Return Loss



(J1 – J3) Insertion Loss and Return Loss



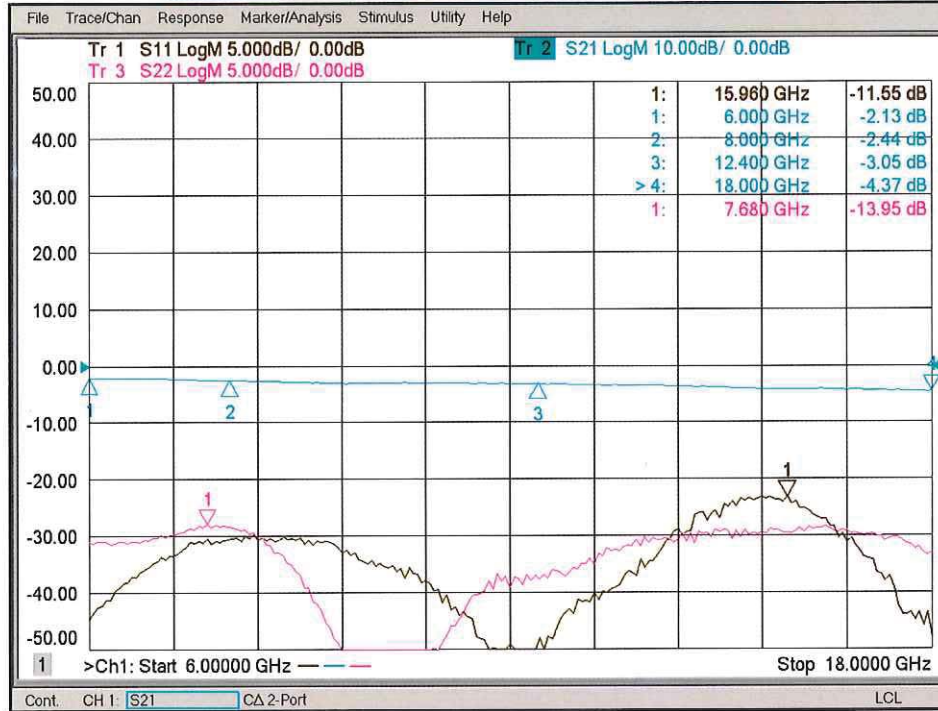
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(J1 – J4) Insertion Loss and Return Loss



(J1 – J5) Insertion Loss and Return Loss



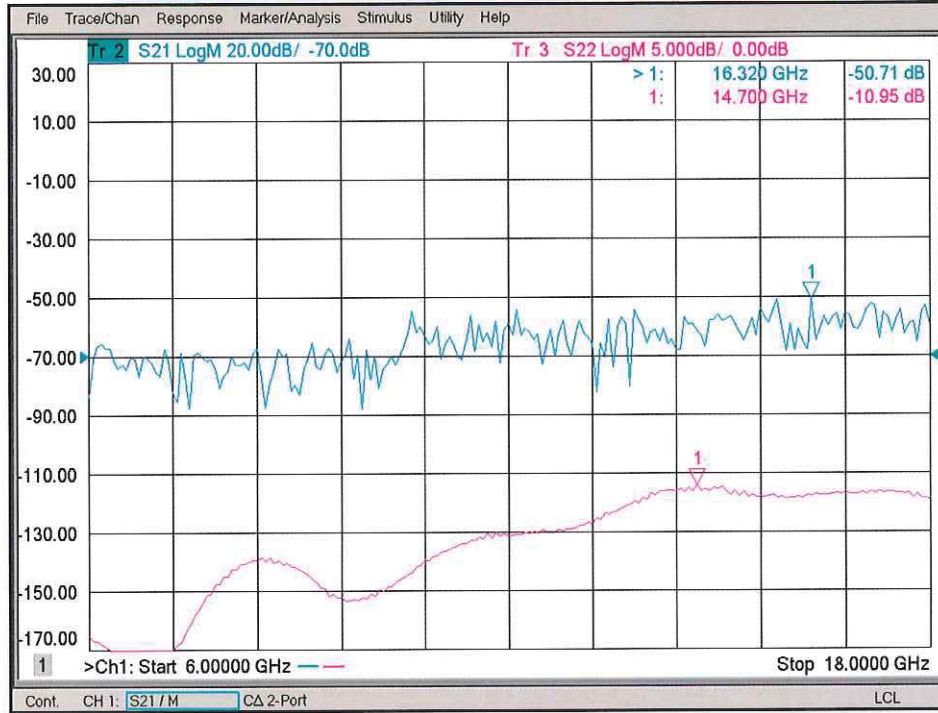
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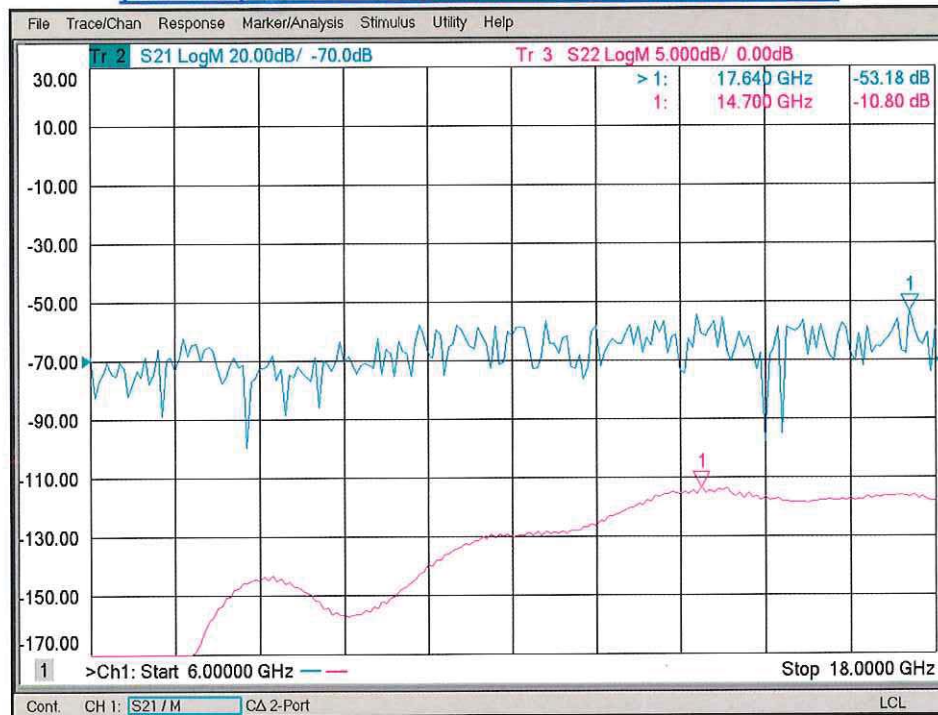
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(J1 – J2) Isolation and Termination Return Loss



(J1 – J3) Isolation and Termination Return Loss



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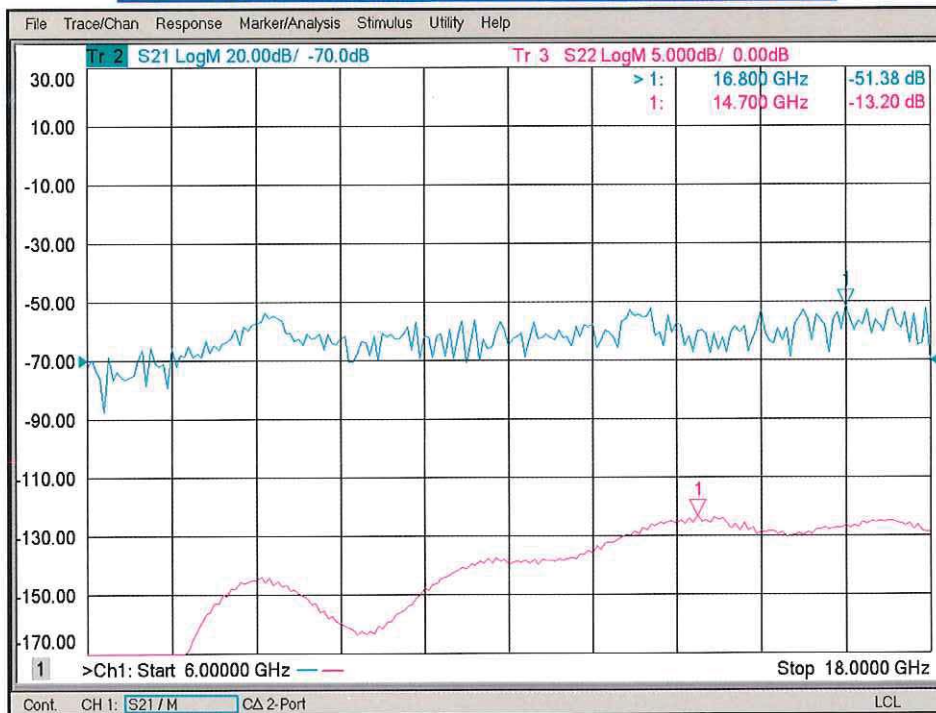
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(J1 – J4) Isolation and Termination Return Loss



(J1 – J5) Isolation and Termination Return Loss



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