A Method for Synthesizing Amplifier Output Networks With Short Circuits at Odd Harmonics and Open Circuits at Even Harmonics for Any Number Of Harmonics

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Abstract—**A method is presented for realizing a network which short circuits the odd harmonics of the fundamental frequency to ground, presents an open circuit at the even harmonics and couples the fundamental frequency to the load. The method is applicable to any number of harmonics.**
   Keywords—**FET, JFET, p-n junctions, pinchoff, amplifiers.**

I. INTRODUCTION

The efficiency of an FET is degraded when the drain voltage is greater than V_{dsat}; the voltage at which pinchoff first occurs. To understand the degradation of the efficiency let us examine the behavior of an FET in saturation. When the drain voltage of a JFET for instance is exactly equal to V_{dsat}, pinchoff occurs exactly at the drain of the transistor as shown in Fig. 1(a) [1]. If the drain voltage is increased by ΔV, the point at which pinchoff occurs moves towards the source a distance of ΔL, as shown in Fig. 1(b). Over the length ΔL the resistance is quite large and the power dissipated in this resistance is equal to the product of the saturated current and ΔV. The voltage ΔV does not contribute to the output power and simply degrades the efficiency. It is therefore clear that, for high efficiency pinchoff needs to be avoided and the depletion region must be minimized. Ideally, for converting DC power to RF power, the channel should have no depletion at all for one-half the cycle and should be completely cut-off for the other one-half cycle. With the optimum load, this should yield the maximum DC-to-RF efficiency. To accomplish this, Grayzel proposed a new FET [2], [3], [4] which will be referred to as the "Grayzel FET".

Fig. 2 shows a simplified schematic of a JFET with a drain voltage of seven volts DC. Points along the channel have values of potential of 0, 1, 2, 3, 4, 5, 6, and 7 V as shown in the figure. The junction is progressively back biased by these potentials, causing greater depletion at the drain than at the source. Fig. 3 shows a simplified schematic diagram of the "Grayzel JFET." The p+ region is divided into N sections that are insulated from one another, forming N, p-n junctions. (In Fig. 3, N is equal to 8 as an illustrative example.) Each p-n junction is biased to ground separately as shown in Fig. 3; the first at V_0 and the eighth at $V_0 + 7$. With a drain voltage of seven volts, all the p-n junctions will have the same DC voltage V_0 across their junctions and hence, to a good approximation the depletion region will be uniform along the channel.
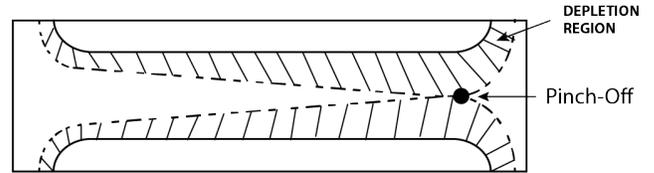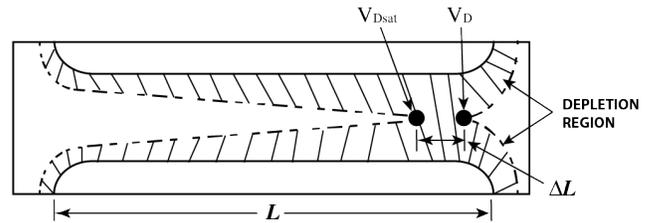

Fig. 1a.

Fig. 1b.

Fig. 1.   The diagrams show the channel of a JFET under different conditions: (a) when the drain voltage equals the pinchoff voltage and (b) when the drain voltage exceeds the pinchoff voltage.
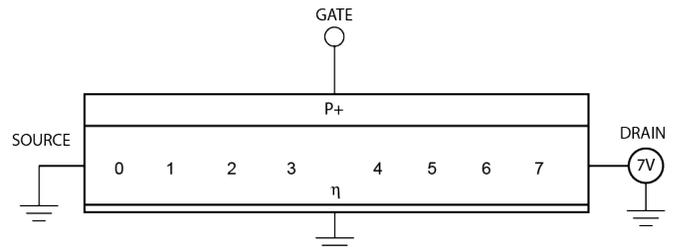

Fig. 2. Voltage Drop Down the Channel of a JFET for a Drain Voltage of 7 Volts.
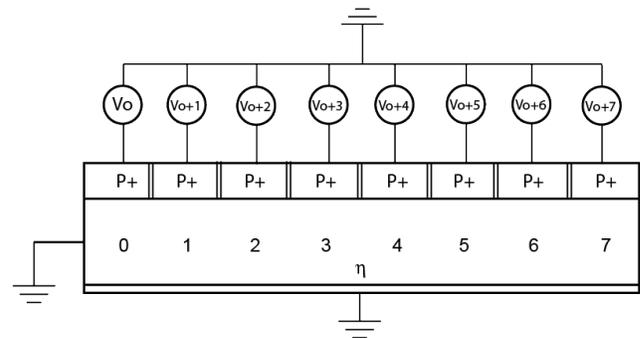

Fig. 3. A "Grayzel JFET" where the p-n junctions are individually biased such that each p-n junction is reverse biased at voltage V_0.

Dividing the gate into multiple sections is applicable to all types of FETs. Fig. 4 shows an example of the "Grayzel MOSFET" with the gate divided into N sections, with N = 6.
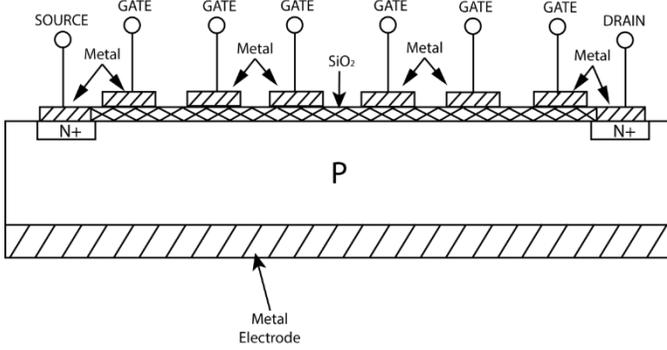

Fig. 4. A simplified schematic of a "Grayzel MOSFET"

Grayzel considered the special case where the odd harmonics are short- circuited and the even harmonics are open-circuited and where for half of the cycle the "Grayzel FET" is cutoff and for the other half of the cycle the depletion region in the channel is of minimal width. The conductance is thus a square wave varying between 0 and G0, where G0 is the conductance when the depletion region in the channel is of minimal width. Fig. 6 shows a plot of the efficiency as a function of X=GL/G0 where GL =1/RL is the conductance of the load presented to the FET.
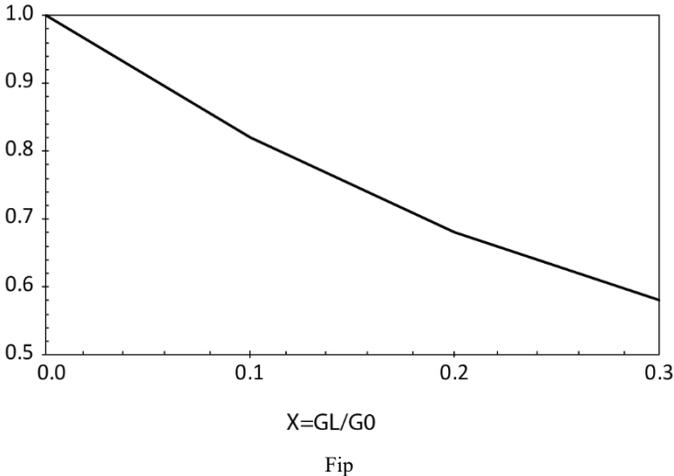

X=GL/G0

Fip

Fig. 5. Efficiency as a function of X

It was found that to approximately achieve this efficiency all harmonics up to and including the eighth need to be terminated. In this paper a synthesis procedure is presented which can synthesize any number of harmonics. Previous art only presents networks which by cut and try methods find networks which only can control the second and third harmonics [5], [6].

II. SYNTHESIS OF THE OUTPUT NETWORK

The output circuit will consist of a shunt reactance followed by a series reactance circuit. The shunt reactance will present a short circuit at the odd harmonics and an open circuit at the fundamental frequency and at the even harmonics. This shunt circuit shorts the odd harmonics as required without affecting the fundamental frequency or the even harmonics. The series reactance will present an open circuit to the even harmonics and a short circuit at the fundamental frequency. Since the odd harmonics have been short circuited to ground the series reactance has no effect on them. The series reactance is realized by a quarter wave open circuited transmission line. It presents a short circuit at the fundamental frequency and an open circuit at the even harmonics. A balun is used to connect it in series. Fig. 6 shows as an example the circuit where N the number of harmonics terminated is equal to eight. A plot of the susceptance $Y(\omega)$ of the shunt reactance circuit is shown in Fig. 7 where the frequency at the fundamental is normalized to $\omega=1$.
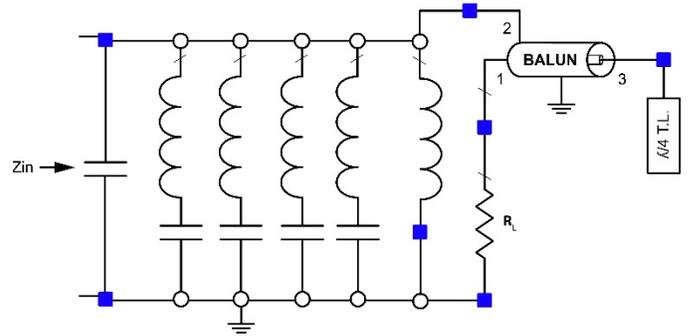

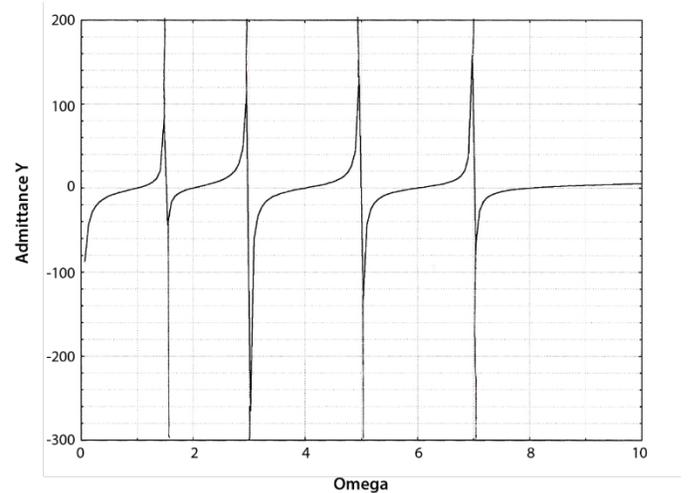Fig. 6. The Amplifier Output Circuit

Fig. 7. The Admittance vs Frequency of the Shunt Circuit

The poles and zeros of a reactance function alternate along the j axis [7]. The zero between the pole at $\omega=1$ and the pole at $\omega=2$ is arbitrary and is set to $\omega=1.5$. The synthesis of this circuit is well known [7]. The reactance is given by Eq. 1 where the fundamental frequency has been normalized with $\omega=1$.

$$Z(s) = K \frac{s(s^2+2.25)(s^2+9)(s^2+25)(s^2+49)}{(s^2+1)(s^2+4)(s^2+16)(s^2+36)(s^2+64)} \tag{1}$$

where s = jω and

$$Y(s) = \frac{(s^2+1)(s^2+4)(s^2+16)(s^2+36)(s^2+64)}{Ks(s^2+2.25)(s^2+9)(s^2+25)(s^2+49)} \quad (2)$$

Y(s) can be expanded in canonical form yielding the parallel connection of a capacitor an inductor and four series resonators as given in Eq. 3.

$$Y(s) = \frac{k_0}{s} + \frac{2k_{1.5}s}{s^2+2.25} + \frac{2k_3 s}{s^2+9} + \frac{2k_5 s}{s^2+25} + \frac{2k_7 s}{s^2+49} + k_\infty s \quad (3)$$

where k_υ are the residues of Y(s) and are equal to

$[(s-s_\upsilon)Y(s)]_{s=s_\upsilon}$ [7].

Using this expression, one finds that $k_0=5.9$, $k_{1.5}= 1.94$ $k_3= 5.35$ $k_5= 4.45$

$k_7= 3.16$ and $k_\infty= 1$. The impedance of each series resonator is given by Eq. 4 when K=1.

$$Z_\upsilon(s) = (s^2 + \omega_\upsilon^2)/2k_\upsilon s = s/2k_\upsilon + 1/(2k_\upsilon/\omega_\upsilon^2)s \quad (4)$$

and $L_\upsilon =1/2k_\upsilon$ and $C_\upsilon =2k_\upsilon/\omega_\upsilon^2$

If the fundamental frequency is f_1 each inductor must be divided by ω and multiplied by K while each capacitor must be divided by ω and by K. K should be chosen to give realizable values for the inductors and capacitors.

III. CONCLUSION

A method has been presented for realizing a network which short circuits the odd harmonics of the fundamental frequency to ground, presents an open circuit at the even harmonics and couples the fundamental frequency to the load. The method is applicable to any number of harmonics. The shunt element is in a canonical form which facilitates tuning the zeros. There is also a shunt capacitor which should include the output capacitance of the transistor. The series resonator consisting of an open circuited transmission line and a balun can be realized in microstrip.

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