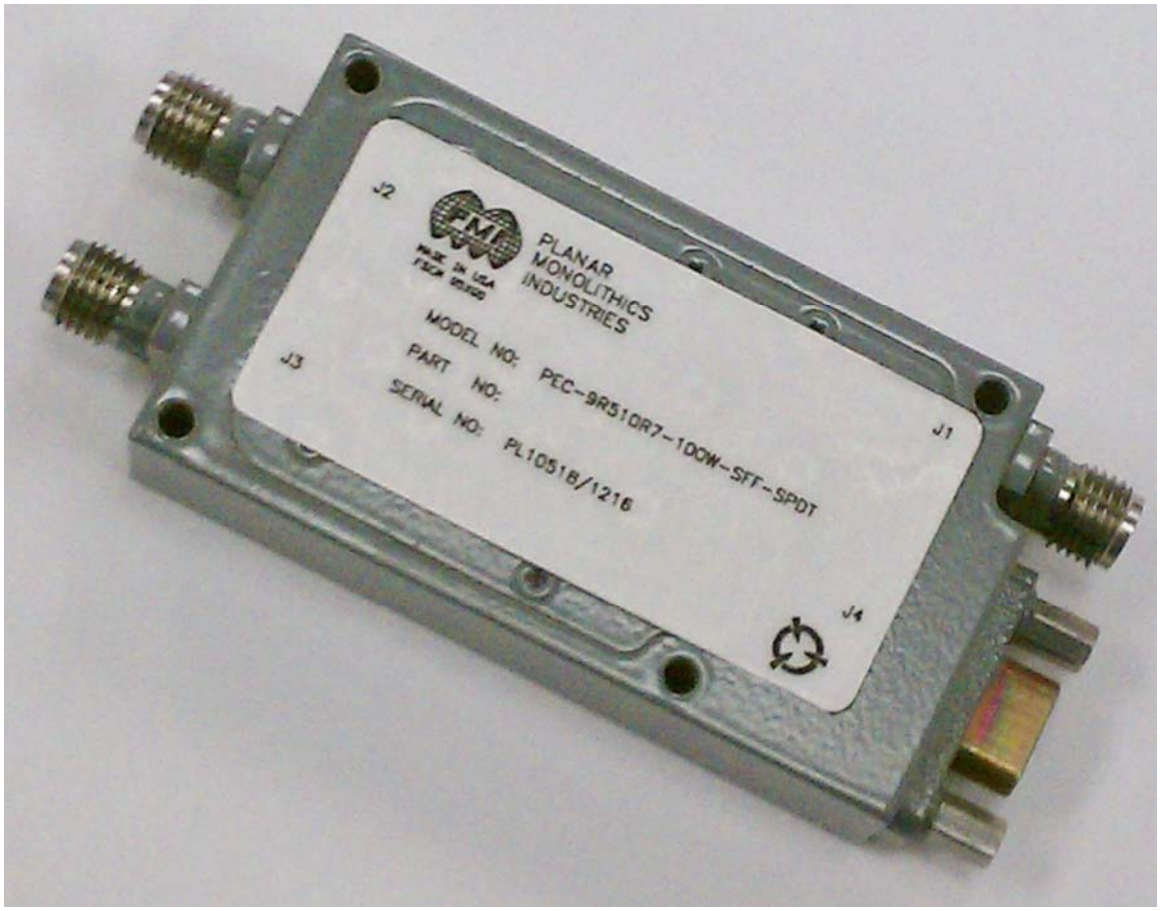
Typical Characteristics
ON
PEC-9R510R7-100W-SFF-SPDT Rev. C



January 24, 2013

Electrical/Thermal Design by: Paul Kuhn & Chuck Newton
Mechanical Design and Drafting by: Nick Ackermann & Simon Kuhn
Tested By: Sebastian Palacio
Reported by: Sebastian Palacio

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This is COLD switch designed to be switched when RF is off. Proper bias levels must be applied when operating this device. Un-used outputs should always be terminated properly.

When you feed high power always feed the common arm (J1) when bias is applied. Never feed the high power into the output (J2 & J3), biased properly or not. Note that if at some point one looses negative biasing while RF power ON, unit will be DAMAGED.

CW signal must be as clean as possible. Preferably a band-pass filter between the signal generator and the TWT to be used in order to eliminate any possible harmonic and sub-harmonic then amplified outside of the operating range of the switch.

1. Mount device onto heat sink with un-painted facing it.
2. Properly terminate un-used RF port. **(MUST)**
3. Apply voltages per outline drawing. Turn power supply on. (All connections must be made)
4. Apply RF power at J1 in increments of 10W and document power output at J2 & J3.
    a. If power drops significantly stop test.
    b. If power stays consistent continue up to 100W-120W.
5. Turn RF power off.
6. Turn power supply off.

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ITEM NO	PARAMETERS	SPECIFIED VALUE	TEST RESULTS	QA QC
1	Frequency Range:	9.5 GHz TO 10.7 GHz	9.5 TO 10.7 GHz	
2	Isolation:	40 dB Min	44.49dB	
3	Insertion Loss:	1.5 dB Typ.	1.34dB	
4	VSWR:	2:1 Typ.	1.42:1	
5	Input Power	100W CW Max	Pass See Certificate	
6	Switching Speed	400ns Max	<300ns See Plots	
7	TTL Control	“1” J1-J2 Insertion Loss “0” J1-J3 Insertion Loss	Pass	
8	DC Power	+5 VDC/500mA Typ. and -28VDC/100mA Typ.	+5V @ 135mA -28V @ 5mA	

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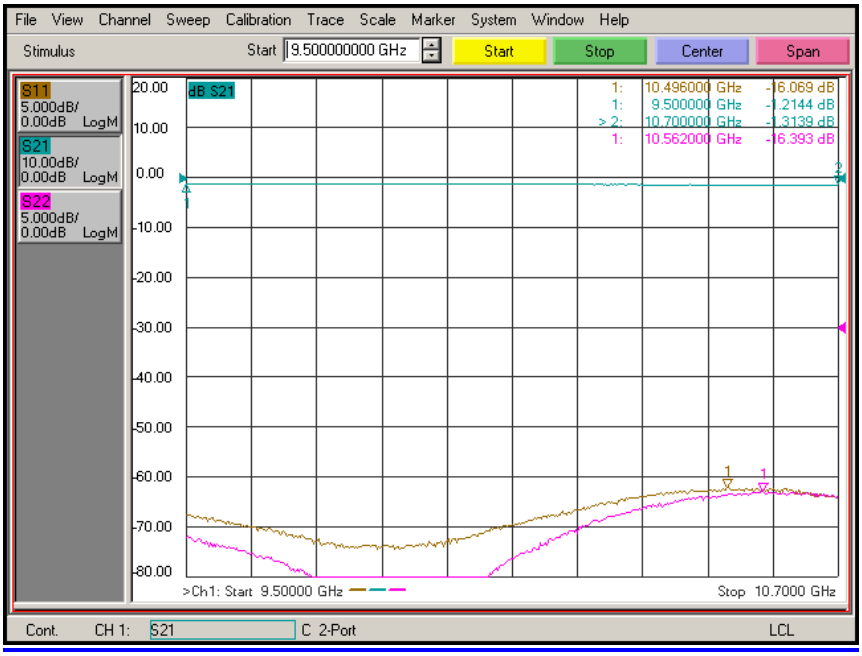
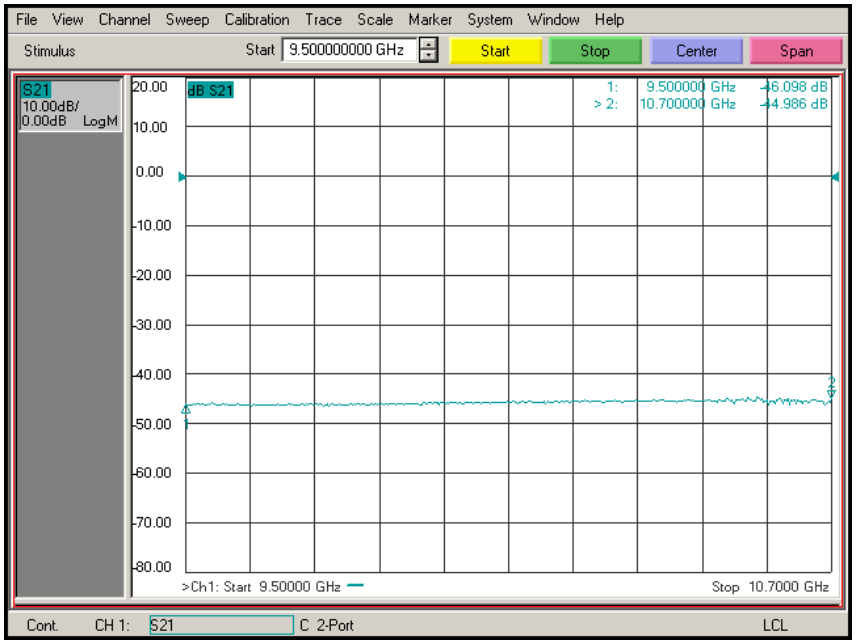
Insertion Loss and Return Loss J1-J2



Isolation J1-J2



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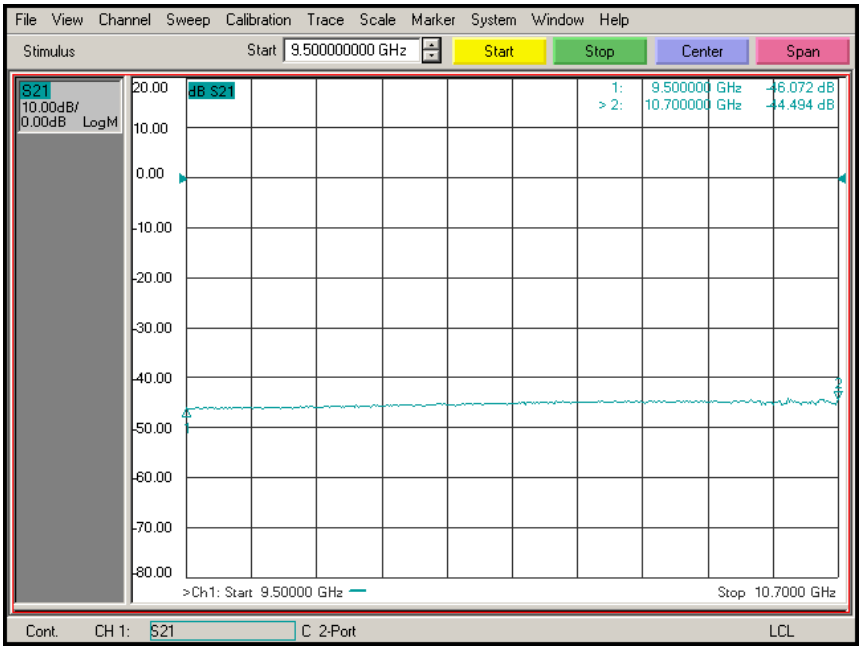
Insertion Loss and Return Loss J1-J3

Isolation J1-J3



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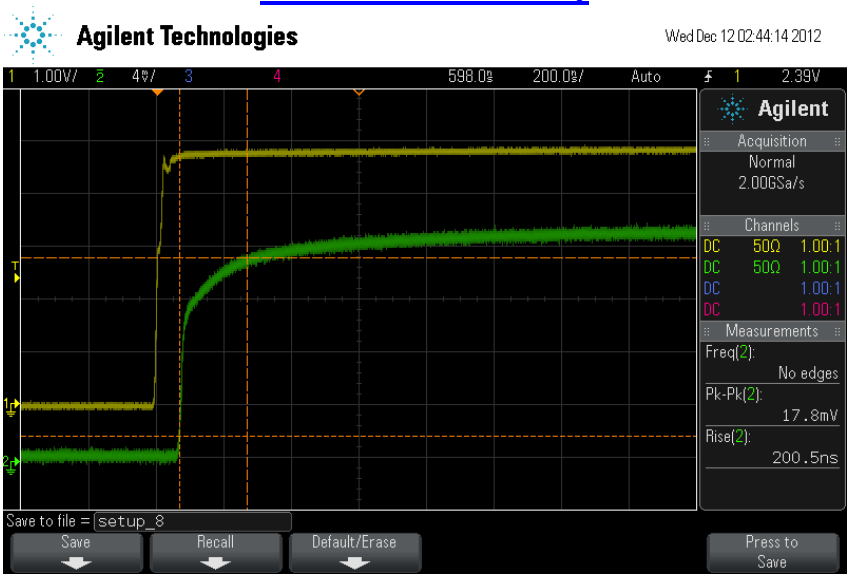
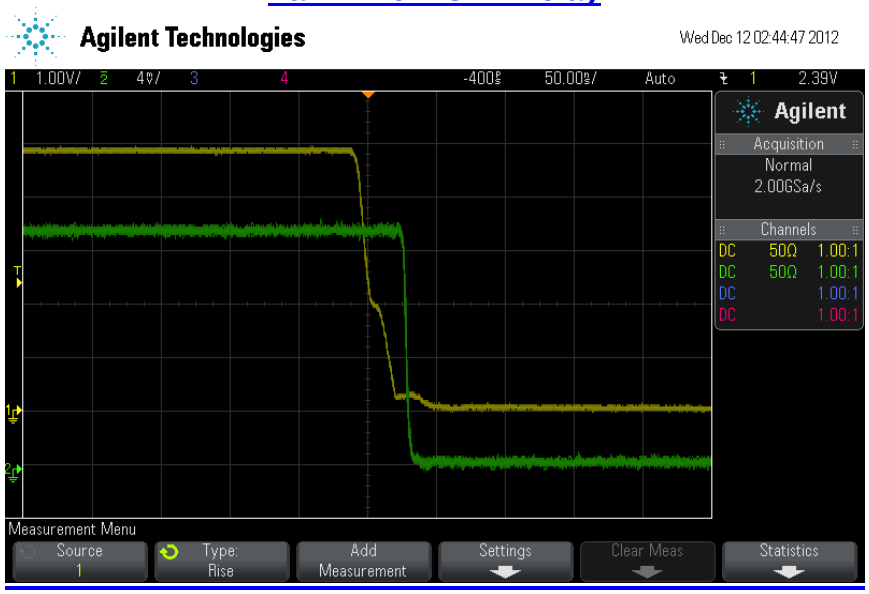
Switching Speed

Rise Time – ON Delay



Fall Time – OFF Delay



Yellow Trace: TTL Signal
Green Trace: RF Signal

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High Power Test Certificate

Millimetrica
RF & Microwave Components–Systems

TEST REPORT N°TRP 230113

P.M.I. HIGH POWER PIN DIODE SWITCH TEST
MOD. PEC-9R510R7-100W-SFF-SPDT (S/N PL10518)

High Power Test at 10.0 GHz

Junction	Inut Power	S21 insertion loss	Consumption Negative Voltage (-28 VDC)	Consumption Positive Voltage (+5 VDC)
	W	dB	mA	mA
J1- J2	10	1.3	1.27	112
J1- J2	20	1.3	1.27	112
J1- J2	30	1.4	1.27	112
J1- J2	40	1.5	1.27	112
J1- J2	50	1.6	1.27	112
J1- J2	60	1.7	1.27	112
J1- J2	70	1.7	1.27	112
J1- J2	80	1.7	1.27	112
J1- J2	90	1.7	1.27	112
J1- J2	100	1.7	1.27	112
J1- J3	10	1.3	1.30	114
J1- J3	20	1.3	1.30	114
J1- J3	30	1.4	1.30	114
J1- J3	40	1.5	1.30	114
J1- J3	50	1.6	1.30	114
J1- J3	60	1.5	1.30	114
J1- J3	70	1.6	1.30	114
J1- J3	80	1.6	1.30	114
J1- J3	90	1.6	1.30	114
J1- J3	100	1.6	1.30	114

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Millimetrica
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Low Power Test
(< +10 dBm Input Drive at 10.0 GHz)

Junction	S11 Input return loss dB	S12 isolation dB	S22 output return loss dB	Rise Time nS	Fall Time nS
J1- J2	15.1	45.2	18.1	<200	<150

Junction	S11 Input return loss dB	S12 isolation dB	S22 output return loss dB	Rise Time nS	Fall Time nS
J1- J3	14.4	45.1	17.0	<100	<350

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