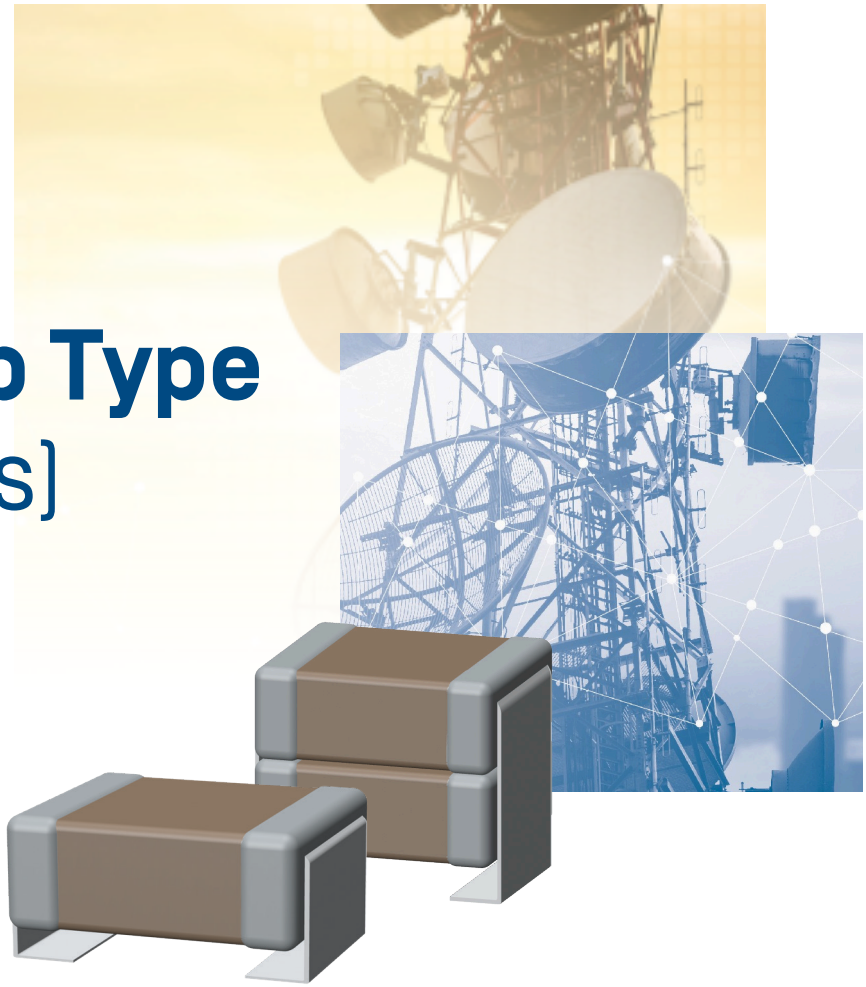
Technical data sheet

MegaCap Type (BC Series)



Quantic UTC's MegaCap Type (BC Series) technology in a leaded and stacked format. Delivering capacitance performance typically associated with much larger footprints. The leaded configuration reduces strain on the part in stressful mechanical and thermal environments. This rugged configuration, coupled with high capacitance values and with available voltages to 1000V makes this an excellent choice for industrial and automotive environments. Available in both C0G and X7R dielectrics, single and multi-chip stacks with J- & L-tab leads. Custom configurations and higher capacitances are also available.

Features

- Higher Capacitance on Same Footprint
- C0G and X7R dielectrics
- Voltages up to 1000V
- High Mechanical & Thermal Endurance
- Excellent Vibration Performance
- AEC-Q200 Options Available
- RoHS Compliant

Applications

Industrial Smoothing & Decoupling

Resonant Charging Systems

DC to DC converters

High Voltage Coupling /DC Blocking

Power Supplies

Snubbers in High Frequency Power Converters

Quantic UTC

RoHS

Quantic UTC is a global capacitor provider manufacturing multilayer ceramic capacitors (MLCCs) and leaded devices for use in defense, aerospace, computer, telecommunications, industrial and various high reliability applications. Our offerings include surface mount (SMT) multi-layer ceramic chip capacitors in both custom and EIA standard sizes; switch mode power supply (SMPS) capacitors in accordance with MIL-PRF-49470 and DSCC/DLA 87106, 88011 drawings and customer source controlled drawings (SCDs); SMT high voltage MLCC; radial leaded high voltage capacitors; SMD large body size MLCC; discoidal capacitors; discoidal arrays; and custom molded case radial parts.

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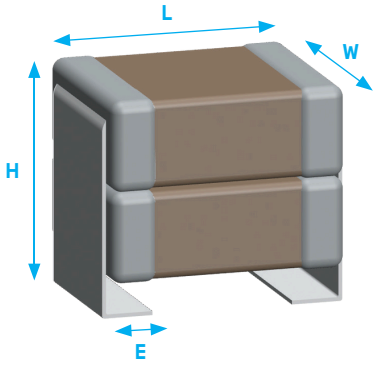
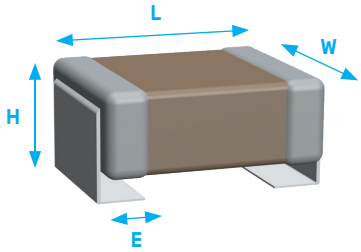
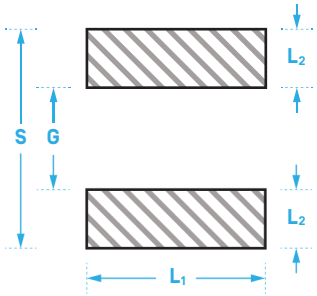
Part Ordering

BC	1	S	2220	J	1	X7R	105	M	T	–	A1N
Series	No. Chip(s)	Voltage Code	Case Code	Lead Type	Coating	Dielectric	Capacitance	Tolerance	Packaging	Test Level	Special Code
MegaCap Type	1 2 3	G = 50VDC B = 100VDC R = 200VDC H = 250VDC S = 500VDC K = 630VDC W = 1000VDC	1210 1812 1825 2220 2225	J = Formed In L = Formed Out	1 = Uncoated	X7R C0G	102 = 1000pF 103 = 10,000pF 223 = 22,000pF 225 = 2,200,000pF (or 2.2µF)	J = ±5% K = ±10% M = ±20%	Tape & Reel Tray		AEC-Q200 = A1N*

*A for AEC-Q200
1 or 0 for product level per AEC-Q200
N for no-coating or C for surface-coating







Standard Dimensions

Landing Pad Dimensions

Case Size	No. Chips	Length [L]	Width [W]	Height [H]	Tab Length [E]	S	L1	L2	G
1210 (3225)	1	0.138±0.016 (3.50±0.40)	0.098±0.016 (2.50±0.40)	*	0.043±0.006 (1.10±0.15)	0.193 (4.90)	0.110 (2.80)	0.055 (1.40)	0.083 (2.10)
	2	N/A	N/A	N/A	N/A				
1812 (4532)	1	0.189±0.016 (4.80±0.40)	0.126±0.016 (3.20±0.40)	*	0.055±0.006 (1.40±0.15)	0.268 (6.80)	0.150 (3.80)	0.063 (1.60)	0.142 (3.60)
	2	0.189±0.016 (4.80±0.40)	0.126±0.016 (3.20±0.40)	*	0.055±0.006 (1.40±0.15)				
1825 (4563)	1	0.189±0.016 (4.80±0.40)	0.248±0.20 (6.30±0.50)	*	0.067±0.006 (1.70±0.15)	0.268 (6.80)	0.268 (6.80)	0.063 (1.60)	0.142 (3.60)
	2	0.189±0.016 (4.80±0.40)	0.248±0.20 (6.30±0.50)	*	0.067±0.006 (1.70±0.15)				
2220 (5750)	1	0.236±0.01 (6.00±0.40)	0.197±0.20 (5.00±0.50)	*	0.067±0.006 (1.70±0.15)	0.331 (8.40)	0.217 (5.50)	0.087 (2.20)	0.157 (4.00)
	2	0.236±0.01 (6.00±0.40)	0.197±0.20 (5.00±0.50)	*	0.067±0.006 (1.70±0.15)				
2225 (5763)	1	0.236±0.01 (6.00±0.40)	0.248±0.020 (6.30±0.50)	*	0.067±0.006 (1.70±0.15)	0.331 (8.40)	0.268 (6.80)	0.087 (2.20)	0.157 (4.00)
	2	0.236±0.01 (6.00±0.40)	0.248±0.020 (6.30±0.50)	*	0.067±0.006 (1.70±0.15)				

*** For height, refer to the individual size/capacitance chart.**

Dialectric Properties & Electrical Summary

Dialectric Case Size	NPO (Class I)	X7R (Class II)
Capacitance1	1210, 1812, 1825, 2220, 2225	
Capacitance	1,000pF to 220,000pF	10,000pF to 47,000,000pF
Tolerance	Single Chip: J(±5%), K(±10%), M(±20%) Two-Chip Stack: M(±20%)	
Rated Voltages (WVDC)	50V, 100V, 200V, 250V, 500V, 630V, 1000V	
Insulation Resistance	≥10GΩ @ 25°C or ≥100GΩ @ 125°C	
Operating Temperature	−55°C to +125°C	
Capacitance Change (TC)	±30ppm/°C	±15%
Dissipation Factor (DF)	0.10% Max	1210 > 4.7µF = 5.0% Max 1812–2225 ≥ 2.2µF = 5.0% Max All other values = 2.5% Max

1. Measured at 1.0 ± 0.2Vrms, 1.0kHz ± 10% for capacitance > 1,000pF.
2. Measured at 25°C and between 30% to 70% relative humidity.

Available Capacitance Values

Case No. Size	Chips	Max Capacitance Rating (µF) for NPO Dialectric							Max Capacitance Rating (µF) for X7R Dialectric							
		50V	100V	200V	250V	500V	630V	Height (H) inch (mm)	50V	100V	200V	250V	500V	630V	1000V	Height (H) inch (mm)
1210	-1	0.039	0.022	0.010	0.010	0.010	0.010	.142±.013 (3.60±0.35)	4.7	3.3	0.7	0.7	0.1	0.1		.142±.013 (3.60±0.35)
	-2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1812	-1	0.100	0.047	0.027	0.027	0.022	0.022	.142±.013 (3.60±0.35)	10.0	4.7	1.0	1.0	0.5	0.2		.142±.013 (3.60±0.35)
	-2	0.220	0.100	0.056	0.056	0.047	0.047	.236±.013 (6.00±0.35)	22.0	10.0	2.2	2.2	1.0	0.5		.236±.013 (6.00±0.35)
1825	-1	0.100	0.100	0.068	0.068	0.047	0.022	.142±.013 (3.60±0.35)	10.0	10.0	1.0	1.0	0.6	0.6		.142±.013 (3.60±0.35)
	-2	0.220	0.220	0.120	0.120	0.100	0.047	.236±.013 (6.00±0.35)	22.0	22.0	2.2	2.2	1.2	1.2		.236±.013 (6.00±0.35)
2220	-1	0.100	0.100	0.068	0.068	0.047	0.022	.142±.013 (3.60±0.35)	22.0	10.0	2.2	2.2	0.5	0.5		.142±.013 (3.60±0.35)
	-2	0.220	0.220	0.120	0.120	0.100	0.047	.236±.013 (6.00±0.35)	47.0	22.0	4.7	4.7	1.0	1.0	1.0	.260±.013 (6.60±0.35)
2225	-1	0.100	0.100	0.100	0.100	0.082	0.068	.142±.013 (3.60±0.35)	10.0	10.0	2.7	2.7	0.6	0.6		.142±.013 (3.60±0.35)
	-2	0.220	0.220	0.220	0.220	0.180	0.120	.236±.013 (6.00±0.35)	22.0	22.0	5.6	5.6	1.2	1.2	0.5	.236±.013 (6.00±0.35)

Test Conditions

1.Visual & Dimensions	Suitable optical or mechanical measurement system	• No major defects • Conforms to individual specification sheet
2.Capacitance	• For capacitance values >1000pF: 1.0±0.2Vrms, 1.0kHz±10% • Measured at room temperature	Shall not exceed specified capacitance plus allowed tolerance
3.DF		NP0: 0.10% Max X7R: • 1210 > 2.2μF = 5.0% Max • 1812 – 2225 ≥ 4.7μF = 5.0% Max • All Other Values = 2.5% Max
4.Dielectric Strength	• Applied voltage: ≦100V : 250% of rated voltage. 100<V≤250V : 200% rated voltage. 250<V≤500V : 150% rated voltage. • Duration: 1 to 5 sec. • Charge & discharge current <50mA.	No evidence of damage or arc-over during test
5.Insulation Resistance	• Time rated voltage applied • ≤100V à max. 120 sec. • >100V à max 60 sec. (Max 500V) • Test at room temperature	≥10GΩ or RxC≥100Ω-F whichever is smaller
6.Temperature Coefficient	• No electrical load • Allow temperature to equilibrate prior to measure	Capacitance change within: • NP0: ±30ppm/°C from -55 to 125°C at 25°C • X7R: ±15% from -55 to 125°C at 25°
7.Termination Adhesion Strength	• Capacitors mounted on a substrate • 10N Force applied central & perpendicular to the device and parallel to the substrate. • Test time: 10±1 sec.	No major damage or removal of termination
8.Vibration Resistance	• Vibration frequency: 10 to 55 Hz cycle • Total amplitude: 1.5mm • Test time: 6 hrs. (Two hrs each in three mutually perpendicular directions.) • Cap./DF Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp	• No major damage • Capacitance change, DF to meet initial specification
9.Solderability	• Solder temperature: 235±5°C • Dipping time: 2±0.5 sec.	95% min. coverage of all metalized area.
10.Bend Test	Force applied to middle of substrate and normal to the substrate surface at a rate of approx. 1mm/s until 1mm deflection achieved, pressure maintained for 5±1 sec.	• No major damage • Capacitance change before and after test within C0G -> ±3.0% or ±2.0pF (whichever is larger). X7R ->within 12.5%
11.Resistance to Soldering Heat	• Solder temperature: 260±5°C • Dipping time: 10±1 sec • Preheating: 120-150°C for 1 min before immersion • Cap. / DF / I.R. Measurement to be made after de-aging at 150°C for 1hr then 24hr age at RT	• No major damage • Capacitance change: within ±2.5% or ±0.25pF whichever is larger. • D.F., I.R. and dielectric strength meet initial spec • 25% max. leaching on each edge

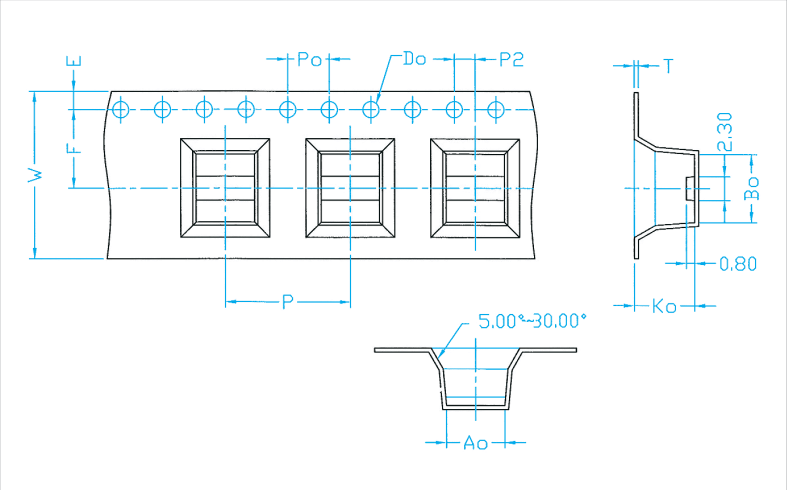
Test Conditions (cont.)

12. Temperature Cycle	• Conduct 5-cycles: 1.Min operating temp: +0/-3°C for 30±3mins 2.Room temp for 2-3mins 3.Max operating temp: +0/-3°C for 30±3mins 4.Room Temp for 2-3 mins • Cap. / DF / I.R. Measurement to be made after de-aging at 150°C for 1hr then 24±2hr age at RT	• No major defects • Cap change: C0G -> within ±2.5% or ±0.25pF whichever is larger. X7R ->within 7.5% • D.F. C0G -> = initial requirement X7R → dF≤150% initial requirement • I.R.: To meet initial requirements
13. Humidity (Steady State)	• Test temp.: 40±2°C • Humidity: 90~95% RH • Test time: 500+24/-0hrs. • Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then 24±2hr age at RT	• No major damage • Cap change: within ±5.0% or ±0.5pF whichever is larger. • D.F. value: ->C0G: 100% of initial requirement ->X7R: dF≤150% of initial requirement • I.R. ≥1GΩ or RC≥50ΩF, whichever is smaller
14. Humidity (Under Load)	• Test temp.: 40±2°C • Humidity: 90~95%RH • Test time: 500+24/-0 hrs. • Applied voltage: rated voltage (MAX. 500V) • Cap. / DF / I.R. Measurement to be made after de-aging at 150°C for 1hr then 24±2hr age at RT	• No major damage • Cap change: C0G ->within ±7.5% or ±0.75pF whichever is larger X7R ->within ±12.5% • I.R.: ≥500MΩ
15. High Temperature Load	• Test temp.: 125±3°C • Applied voltage: 1. ≤100V: 200% rated voltage. 2. 100<V≤500: 150% rated voltage. 3. ≧630V: 120% rated voltage. Exceptions (X7R 0nly): 1. All parts Cap≥10μF, All parts ≤100V & ≥1μF: 150% rated voltage 2. 2220 ≥100V, ≥15μF: 120% rated voltage 3. 1210 ≥100V, ≥3.3μF: 100% rated voltage • Test time: 1000+24/-0 hrs. • Cap. / DF / I.R. Measurement to be made after de-aging at 150°C for 1hr then 24±2hr age at RT	• No major damage • Cap change: C0G ->within ±3.0% or ±0.3pF whichever is larger X7R -> within ±12.5% • D.F. value: ->: dF≤200% of initial requirement • I.R. ≥1GΩ or RC≥50ΩF, whichever is smaller
"Room Temperature" or "RT" equivalent to 15°C to 35°C; Relative humidity 25% to 75%; Atmospheric pressure 86kPa to 106kPa.		

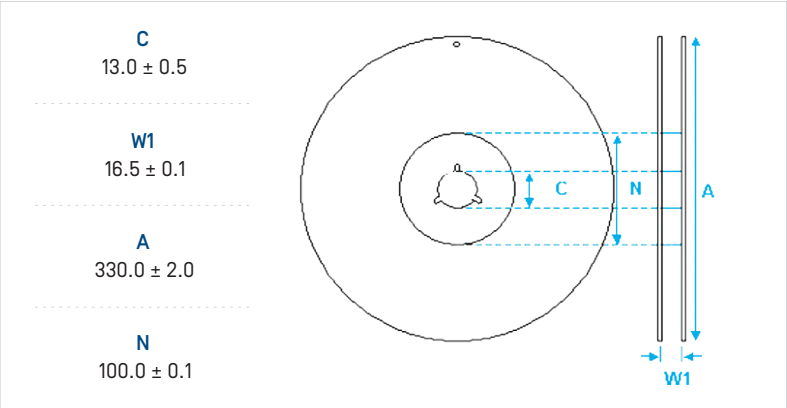
Packaging Dimensions & Part Count

Size	1210 & 1812 Single Chip	All Other Sizes
A_0	Varies	Varies
B0	Varies	Varies
K_0	Varies	Varies
W	16.00±0.30mm	16.00±0.30mm
E	1.75±0.10mm	1.75±0.10mm
F	7.50±0.10mm	7.50±0.10mm
P	8.00±0.10mm	12.00±0.10mm
T	0.40±0.05mm	0.40 or 0.50±0.05mm
P0	4.00±0.10mm	
10×P0	40.00±0.10mm	
P2	2.00±0.05mm	
D0	Ø1.50+0.10/−0.00mm	

Plastic Tape Dimensions



Reel Dimensions 13"



Chip Size	1210	1812		1825		2220		2225	
No. Chips	1	1	2	1	2	1	2	1	2
Parts per 13" Reel	1.5K	1.5K	0.5K	1K	0.5K	1K	0.5K	Enquire	

Storage & Handling Conditions

- Parts should be stored in their original packing where possible. Temperature should be between 5°C and 40°C. Relative humidity maintained between 20% to 70%
- Do not store in the presence of salts, hydrogen sulfide, sulfur dioxide, chloride gas, ammonia or other acid and alkali.
- It is recommended that the product be used within one year of receipt. Check solderability in case shelf-life extension is needed.
- Parts should be handled with care. If product is dropped it should be discarded even of cracks can not be observed on the exterior of the device.

Soldering Conditions

MegaCap Type (BC Series) are suitable for a range of soldering methods. However, care must be taken not to thermally shock the ceramic chip. Reflow profiles should not exceed 2°C per second in both the heating and cooling stages. The maximum temperature during reflow must not exceed 260°C. It is possible to hand-solder leaded devices. Chips should be pre-heated to within 25°C to 50°C of reflow temperature. Use of a soldering iron rated no more than 30 Watts is recommended. The tip of the soldering iron should be placed on the circuit board landing pad rather than the capacitor lead. At no point should the tip of the soldering iron make contact with the ceramic capacitor body or termination.